Course/Branch : B.E/CSE	**Year / Semester** : III/V	Format No.	NAC/TLP-07a.13
Subject Code :EC8691	**Subject Name** :Microprocessor &Microcontroller	Rev. No.	02
Unit No : I	**Unit Name** **:** The 8086 Microprocessor	Date	30.09.2020

OBJECTIVE TYPE QUESTION BANK

S. No.	Objective Questions (MCQ /True or False / Fill up with Choices)	BTL
1	8086 Microprocessor supports _____ modes of operation. A) **2** B) 3 C) 4 D) 5	L5
2	Which of the following is not a Features of 8086? A) It uses two stages of pipelining B) It is available in 3 versions based on the frequency of operation C) Fetch stage can pre fetch up to 6 bytes of instructions D) **It has 512 vectored interrupts**.	L5
3	It is an edge triggered input, which causes an interrupt request to the microprocessor. A) **NMA** B) INTR C) INTA D) ALE	L5
4	Which flag represents the result when the system capacity is exceeded? A) Carry flag B) Auxiliary flag C) Trap flag D) Overflow flag	L5
5	It is used to write the data into the memory or the output device depending on the status of M/IO signal. A) IR B) HLDA C) HR D) **WR**	L5
6	The instruction, MOV AX, 1234H is an example of A) Register addressing mode B) Direct addressing mode C) **Immediate addressing mode** D) Based indexed addressing mode	L5

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7	If the data is present in a register and it is referred using the particular register, then it is a) direct addressing mode **b) register addressing mode** c) indexed addressing mode d) immediate addressing mode	L5
8	The contents of a base register are added to the contents of index register in A) Indexed Addressing Mode B) Based Indexed Addressing Mode C) Relative Based Indexed Addressing Mode **D) Based Indexed And Relative Based Indexed Addressing Mode**	L5
9	If the location to which the control is to be transferred lies in a different segment other than the current one, then the mode is called A) Intra Segment Mode B) Intersegment Direct Mode C) Intersegment Indirect Mode D) **Intersegment Direct And Indirect Mode**	L5
10	The instruction that is used to transfer the data from source operand to destination operand is **A) Data Copy/Transfer Instruction** B) Branch Instruction C) Arithmetic/Logical Instruction D) String Instruction	L5
11	The instructions that involve various string manipulation operations are A) Branch Instructions B) Flag Manipulation Instructions C) Shift And Rotate Instructions **D) String Instructions**	L5
12	The instruction that pushes the contents of the specified register/memory location on to the stack is A) PUSHF B) POPF **C) PUSH** D) POP	L5

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13	The instructions that are used for reading an input port and writing an output port respectively are A) MOV, XCHG B) MOV, IN C) IN, MOV **D) IN, OUT**	
14	The instruction that adds immediate data/contents of the memory location specified in an instruction/register to the contents of another register/memory location is A) SUB **B) ADD** C) MUL D) DIV	L5
15	When the CPU executes IRET, **A) Contents Of IP And CS Are Retrieved** B) The Control Transfers From ISR To Main Program C) Clears The Trap Flag D) Clears The Interrupt Flag	L5
16	At the end of ISR, the instruction should be A) END B) ENDS **C) IRET** D) INTR	L5
17	The type of the interrupt may be passed to the interrupt structure of CPU from A) Interrupt Service Routine B) Stack **C) Interrupt Controller** D) None Of The Mentioned	L5
18	The interrupt request that is independent of IF flag is A) NMI B) TRAP C) Divide By Zero **D) All Of The Mentioned**	L5

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19	The instruction that performs logical AND operation and the result of the operation is not available is A) AAA B) AND **C) TEST** D) XOR	L5
20	In the RCL instruction, the contents of the destination operand undergo function as **A) Carry Flag Is Pushed Into LSB & MSB Is Pushed Into The Carry Flag** B) Carry Flag Is Pushed Into MSB & LSB Is Pushed Into The Carry Flag C) Auxiliary Flag Is Pushed Into LSB & MSB Is Pushed Into The Carry Flag D) Parity Flag Is Pushed Into MSB & LSB Is Pushed Into The Carry Flag	L5
21	The instruction that is used as prefix to an instruction to execute it repeatedly until the CX register becomes zero is A) SCAS **B) REP** C) CMPS D) STOS	L5
22	The instructions that are used to call a subroutine from the main program and return to the main program after execution of called function are A) CALL, JMP B) JMP, IRET **C) CALL, RET** D) JMP, RET	L5
23	NOP instruction introduces A) Address **B) Delay** C) Memory Location D) None Of The Mentioned	L5
24	The directive used to inform the assembler, the names of the logical segments to be assumed for different segments used in the program is **A) ASSUME** B) SEGMENT C) SHORT	L5

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	D) DB	
25	The directive that marks the end of an assembly language program is A) ENDS **B) END** C) ENDS & END D) None Of The Mentioned	L5
26	The directive that updates the location counter to the next even address while executing a series of instructions is A) EVN **B) EVEN** C) EVNE D) EQU	L5
27	The labels or constants that can be used by any module in the program is possible when they are declared as A) PUBLIC B) LOCAL **C) GLOBAL** D) EITHER PUBLIC OR GLOBAL	L5
28	While CPU is executing a program, an interrupt exists then it A) Follows The Next Instruction In The Program B) Jumps To Instruction In Other Registers **C) Breaks The Normal Sequence Of Execution Of Instructions** D) Stops Executing The Program	L5
29	An Interrupt Breaks The Execution Of Instructions And Diverts Its Execution To **A) Interrupt Service Routine** B) Counter Word Register C) Execution Unit D) Control Unit	L5
30	While executing the main program, if two or more interrupts occur, then the sequence of appearance of interrupts is called A) Multi-Interrupt B) Nested Interrupt	L5

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	C) Interrupt Within Interrupt **D) Nested Interrupt And Interrupt Within Interrupt**	
31	Whenever a number of devices interrupt a CPU at a time, and if the processor is able to handle them properly, it is said to have A) Interrupt Handling Ability B) Interrupt Processing Ability **C) Multiple Interrupt Processing Ability** D) Multiple Interrupt Executing Ability	L5
32	NMI stands for **A) Nonmaskable Interrupt** B) Nonmultiple Interrupt C) Nonmovable Interrupt D) None Of The Mentioned	L5
33	If any interrupt request given to an input pin cannot be disabled by any means then the input pin is called A) Maskable Interrupt **B) Nonmaskable Interrupt** C) Maskable Interrupt And Nonmaskable Interrupt D) None Of The Mentioned	L5
34	The INTR interrupt may be **A) Maskable** B) Nonmaskable C) Maskable And Nonmaskable D) None Of The Mentioned	L5
35	The Programmable interrupt controller is required to A) Handle One Interrupt Request **B) Handle One Or More Interrupt Requests At A Time** C) Handle One Or More Interrupt Requests With A Delay D) Handle No Interrupt Request	L5
36	If a number of instructions are repeating through the main program, then to reduce the length of the program, _____ is used.	L5

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	A) Procedure B) Subroutine **C) Macro** D) None Of The Mentioned	
37	The process of assigning a label or macro name to the string is called A) Initializing Macro B) Initializing String Macro C) Defining A String Macro **D) Defining A Macro**	L5
38	Inserting the statements and instructions represented by macro, directly at the place of the macro name, in the program, is known as **A) Calling A Macro** B) Inserting A Macro C) Initializing A Macro D) None Of The Mentioned	L5
39	The stack pointer register contains A) Address Of The Stack Segment B) Pointer Address Of The Stack Segment **C) Offset Of Address Of Stack Segment** D) Data Present In The Stack Segment	L5
40	The register or memory location that is pushed into the stack at the end must be A) Popped Off Last B) Pushed Off First **C) Popped Off First** D) Pushed Off Last	L5