Course/Branch : B.E / CSE	**Year / Semester** : III/V	Format No.	NAC/TLP-07a.13
Subject Code : EC8691	**Subject Name** :Microprocessor&Microcontroller	Rev. No.	02
Unit No : II	**Unit Name** : 8086 System Bus Structure	Date	30.09.2020

OBJECTIVE TYPE QUESTION BANK

S. No.	Objective Questions (MCQ /True or False / Fill up with Choices)	BTL
1	AD0-AD15 pins will act as address bus when **A)ALE Is Set To 1** B)ALE Is Set To 0 C)BHE Pin Is Enabled D BHE Pin Is Disabled	L2
2	In 8086, in maximum mode, there can be more than one microprocessor in the system configuration. **A) True** B) False	L2
3	Data bus bits D8-D15 are enabled only if **A)BHE Pin Is Enabled** B) BHE Pin Is Disabled C) ALE Is Set To 1 D)ALE Is Set To 0	L2
4	In 8086, Maximum mode is designed to be used when a coprocessor (8087) exists in the system **A)True** B)False	L2
5	The clock rate of microprocessor 8086 is _____. A) 5 MHZ B) 8 MHZ C) 10 MHZ **D) All of The Mentioned**	L2
6	In which T-state does the CPU send the address to memory or I/O and the ALE signal for demultiplexing _____ . **A) T1** B) T2 C) T3 D) T4	L2

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7	BHE of 8086 microprocessor signal is used to interface the_____ A) I/O B) DMA C) Even Bank Memory **D) Odd Bank Memory**	L2
8	Ready pin of a microprocessor is used_____ A) To Indicate That Processor Is Ready to Receive Inputs Outputs B) To Indicate That Processor Is Ready to Receive Inputs Output **C) To Introduce Wait States** D) To Provide Direct Memory Access.	L2
9	The pins of minimum mode AD0-AD15 have _____ address and ____ data bus. A) 16, 8 **B) 16, 16** C) 8, 16 D) 8, 8	L2
10	The function of pins from 24 to 31 depend on the mode in which ____ is operating. A) 80386 B) 80387 C) 8085 **D) 8086**	L2
11	The _____ input is examined by a 'wait' instruction. A) K **B) TEST** C) LOC D) KIT	L2
12	After reset execution starts form _____. a) 00000H **b) FFFF0H** c) FFFFFH d) 003FFH	L2
13	If there is an edge triggered input at NMI Pin causes_____ Interrupt. A) Type-0	L2

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	B) Type-1 **C) Type-2** D) Type-3	
14	If MN/MX is low, the 8086 operates in _____ mode. A) Minimum Mode **B) Maximum Mode** C) Both A and B D) Control Mode	L2
15	The RD, WR, M/IO is the heart of control for a _____ mode. **A) Minimum Mode** B) Maximum Mode C) Both A and B D) Control Mode	L2
16	If S'_2 =0, S'_1 =1, S'_0 =1, what is the status of the microprocessor? A) Interrupt Acknowledge B) Read I/O Port C) Write I/O Port **D) Halt**	L2
17	Which of the following processor supports pipelined architecture? A) 8080 B) 8085 **C) 8086** D) 8008	L2
18	In order to initiate the fetch cycle by BIU at least _____ bytes of the queue must be empty. A) 1 **B) 2** C) 3 D) 4	L2
19	The interrupt for which the processor has the highest priority among all the external interrupts is A) Keyboard Interrupt B) TRAP **C) NMI**	L2

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	D) INT	
20	A _____is a set of instructions which is prepared to perform a specific assignment if executed by a computer. A) Browser B) Internet **C) Program** D) Code	L2
21	A program is an active entity. A) True **B) False**	L2
22	A technique that allows more than one program to be ready for execution and provides the ability to switch from one process to another. A) Multitasking B) Multiprocessing C) Multitasking **D) Multiprogramming**	L2
23	Multiprogramming is mainly accomplished by: **A) OS** B) Software C) Hardware D) Program	L2
24	The technique that increases the system's productivity. A) Multiprogramming B) Multitasking C) Multiprocessing D) **Single-Programming**	L2
25	What does 'b' represent in a processor wait ratio? A) Input Ratio B) Output Ratio C) Average Time **D) Average I/O Time**	L2

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26	Processor wait ratio is given by _____ A) W=B/E+B **B) W=B/E-B** C) #=B/E-B D) #=B/E+B	L2
27	This cycle, of going through _____ states of running and input/output, may be repeated over and over until the job is completed. A) Evaluation **B) Process** C) Program D) Data	L2
28	How many types of basic multiprocessor configurations? A) 2 **B) 3** C) 4 D) 5	L2
29	A _____ is a specially designed circuit on microprocessor chip which can perform the same task very quickly, which the microprocessor performs **A) Coprocessor configuration** B) Closely coupled configuration C) Loosely coupled configuration D) None of the above	L2
30	The coprocessor and the processor is connected via? A) TEST B) QS0 C) QS1 **D) All of the above**	L2
31	_____signal takes care of the coprocessor's activity, i.e. the coprocessor is busy or idle. **A) TEST** B) QS0 C) QS1 D) None of the above	L2

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32	Which of the following are advantage of Loosely Coupled Configuration? A) Having more than one processor results in increased efficiency. B) easy to achieve parallel processing. C) system structure is flexible **D) All of the above**	L2
33	8087 numeric data processor is also known as? A) Math co-processor B) Numeric processor extension C) Floating point unit **D) All of the above**	L2
34	8087 Architecture is divided into? A) 2 **B) 3** C) 4 D) 5	L2
35	It is a power supply signal, which requires +5V supply for the operation of the circuit. A) VCA B) VDD **C) VCC** D) INTA	L2
36	The _____ handles all the communication between the processor and the memory A) Numeric Extension Unit B) Packed Unit **C) Control Unit** D) Binary Unit	L2
37	8087 Numeric Data Processor designed by? **A) Intel** B) IBM C) Microsoft D) VAX	L2

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38	The number of instructions actually executed by the microprocessor depends on the A) Stack **B) Loop Count** C) Program Counter D) Time Duration	L2
39	In case of subroutines, the actual number of instructions executed by the processor depends on A) Loop Count B) Length Of Interrupt Service Routine **C) Length Of Procedure** D) None	L2
40	When large delays are required, then to serve the purpose **A) One Or More Count Registers Can Be Used** B) One Or More Shift Registers Can Be Used C) One Or More Pointer Registers Can Be Used D) One Or More Index Registers Can Be Used	L2