Course/Branch : B.E./CSE	**Year / Semester** :II/III	Format No.	NAC/TLP-07a.13
Subject Code :CS8351	**Subject Name** :Digital Principles and System Design	Rev. No.	02
Unit No :3	**Unit Name** :**Synchronous Sequential logic**	Date	30.09.2020

OBJECTIVE TYPE QUESTION BANK

S. No.	Objective Questions (MCQ /True or False / Fill up with Choices)	BTL
1	Latch is a device with _____ a) One stable state b) **Two stable state** c) Three stable state d) Infinite stable states	L2
2	A latch is an example of a _____ a) Monostable multivibrator b) Astable multivibrator c) **Bistable multivibrator** d) 555 timer	L2
3	How many types of latches are _____ a) **4** b) 3 c) 2 d) 5	L4
4	The full form of SR is _____ a) System rated b) **Set reset** c) Set ready d) Set Rated	L5
5	The outputs of SR latch are _____ a) x and y b) a and b c) s and r d) **q and q'**	L1
6	The truth table for an S-R flip-flop has how many VALID entries? a) 1 b) 2 c) **3** d) 4	L2
7	The logic circuits whose outputs at any instant of time depends only on the present input but also on the past outputs are called a) Combinational circuits b) **Sequential circuits** c) Latches d) Flip-flops	L2
8	How many types of sequential circuits are? a) **2** b) 3 c) 4 d) 5	L4

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9	In S-R flip-flop, if Q = 0 the output is said to be _____ a) Set b) **Reset** c) Previous state d) Current state	L5
10	What is a trigger pulse? a) **A pulse that starts a cycle of operation** b) A pulse that reverses the cycle of operation c) A pulse that prevents a cycle of operation d) A pulse that enhances a cycle of operation	L1
11	A basic S-R flip-flop can be constructed by cross-coupling of which basic logic gates? a) AND or OR gates b) XOR or XNOR gates c) **NOR or NAND gates** d) AND or NOR gates	L2
12	Whose operations are faster among the following? a) **Combinational circuits** b) Sequential circuits c) Latches d) Flip-flops	L2
13	The basic latch consists of _____ a) **Two inverters** b) Two comparators c) Two amplifiers d) Two adders	L4
14	When is a flip-flop said to be transparent? a) When the Q output is opposite the input b) **When the Q output follows the input** c) When you can see through the IC packaging d) When the Q output is complementary of the input	L5
15	What is one disadvantage of an S-R flip-flop? a) It has no Enable input b) It has a RACE condition c) It has no clock input d) **Invalid State**	L1
16	The characteristic equation of S-R latch is _____ a) **Q(n+1) = (S + Q(n))R'** b) Q(n+1) = SR + Q(n)R c) Q(n+1) = S'R + Q(n)R d) Q(n+1) = S'R + Q'(n)R	L2
17	How is a J-K flip-flop made to toggle? a) J = 0, K = 0	L2

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	b) J = 1, K = 0 c) J = 0, K = 1 d) **J = 1, K = 1**	
18	In J-K flip-flop, "no change" condition appears when _____ a) J = 1, K = 1 b) J = 1, K = 0 c) J = 0, K = 1 d) **J = 0, K = 0**	L4
19	What is the significance of the J and K terminals on the J-K flip-flop? a) There is no known significance in their designations b) The J represents "jump," which is how the Q output reacts whenever the clock goes high and the J input is also HIGH c) **The letters were chosen in honour of Jack Kilby, the inventory of the integrated circuit** d) All of the other letters of the alphabet are already in use	L5
20	The asynchronous input can be used to set the flip-flop to the _____ a) 1 state b) 0 state c) **either 1 or 0 state** d) forbidden State	L1
21	In JK flip flop same input, i.e. at a particular time or during a clock pulse, the output will oscillate back and forth between 0 and 1. At the end of the clock pulse the value of output Q is uncertain. The situation is referred to as? a) Conversion condition b) **Race around condition** c) Lock out state d) Forbidden State	L2
22	Master slave flip flop is also referred to as? a) Level triggered flip flop b) **Pulse triggered flip flop** c) Edge triggered flip flop d) Edge-Level triggered flip flop	L2
23	S-R type flip-flop can be converted into D type flip-flop if S is connected to R through _____ a) OR Gate b) AND Gate c) **Inverter** d) Full Adder	L4
24	The term synchronous means _____ a) The output changes state only when any of the input is triggered b) **The output changes state only when the clock input is triggered** c) The output changes state only when the input is reversed d) The output changes state only when the input follows it	L5

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25	The S-R, J-K and D inputs are called _____ a) Asynchronous inputs b) **Synchronous inputs** c) Bidirectional inputs d) Unidirectional inputs	L1
26	A counter circuit is usually constructed of _____ a) A number of latches connected in cascade form b) A number of NAND gates connected in cascade form c) **A number of flip-flops connected in cascade** d) A number of NOR gates connected in cascade form	L2
27	What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops? a) 0 to 2^n b) 0 to $2^n + 1$ c) **0 to $2^n - 1$** d) 0 to $2^{n+1/2}$	L2
28	Ripple counters are also called _____ a) SSI counters b) **Asynchronous counters** c) Synchronous counters d) VLSI counters	L4
29	BCD counter is also known as _____ a) Parallel counter b) **Decade counter** c) Synchronous counter d) VLSI counter	L5
30	How many natural states will there be in a 4-bit ripple counter? a) 4 b) 8 c) **16** d) 32	L1
31	Internal propagation delay of asynchronous counter is removed by _____ a) Ripple counter b) Ring counter c) Modulus counter d) **Synchronous counter**	L2
32	How many flip-flops are required to construct a decade counter? a) **4** b) 8 c) 5 d) 10	L2
33	A 5-bit asynchronous binary counter is made up of five flip-flops, each with a 12 ns propagation delay. The total propagation delay (tp(total)) is _____	L4

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	a) 12 ms b) 24 ns c) 48 ns d) **60 ns**	
34	A down counter using n-flip-flops count _____ a) **Downward from a maximum count** b) Upward from a minimum count c) Downward from a minimum to maximum count d) Toggles between Up and Down count	L5
35	UP Counter is _____ a) **It counts in upward manner** b) It count in down ward manner c) It counts in both the direction d) Toggles between Up and Down count	L1
36	A register is defined as _____ a) The group of latches for storing one bit of information b) The group of latches for storing n-bit of information c) The group of flip-flops suitable for storing one bit of information d) **The group of flip-flops suitable for storing binary information**	L2
37	How many types of registers are? a) 2 b) 3 c) **4** d) 5	L2
38	In D register, 'D' stands for _____ a) Delay b) Decrement c) **Data** d) Decay	L4
39	Registers capable of shifting in one direction is _____ a) Universal shift register b) **Unidirectional shift register** c) Unipolar shift register d) Unique shift register	L5
40	A shift register is defined as _____ a) The register capable of shifting information to another register b) **The register capable of shifting information either to the right or to the left** c) The register capable of shifting information to the right only d) The register capable of shifting information to the left only	L1