Course/Branch : B.E./CSE	**Year / Semester** :II/III	Format No.	NAC/TLP-07a.13
Subject Code :CS8351	**Subject Name** :Digital Principles and System Design	Rev. No.	02
Unit No :4	**Unit Name** :**Asynchronous Sequential logic**	Date	30.09.2020

OBJECTIVE TYPE QUESTION BANK

S. No.		BTL
1	Asynchronous circuits are useful in application where the input signals may a. change at any time b. never change c. **both a and b** d. None	L2
2	Table that is not a part of asynchronous analysis procedure is a. transition table b. state table c. flow table d. **excitation table**	L2
3	The making of transition table consists of a. 2 steps b. 4 steps c. 5 steps d. **6 steps**	L4
4	In asynchronous circuit, the changes occur with the change of a. **input** b. output c. clock pulse d. time	L5
5	In synchronous circuits, present state is determined by a. Unclocked flip-flops b. clocked flip-flops c. **flip-flops** d. latches	L1
6	The present states and next state of asynchronous circuits are also called a. **secondary variables** b. primary variables c. excitation variables d. short term memory	L2
7	The race in which stable state depends on order is called a. **critical race** b. identical race c. non critical race d. defined race	L2
8	Unclocked flip-flops are called a. **Latches** b. register c. Transition tables d. None	L4
9	In primitive flow table for gated latch, each state has a. **1 row**	L5

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	b. 2 rows c. 3 rows d. 4 rows	
10	The complexity of asynchronous circuit is involved in timing problems of a. inputs b. outputs c. clock pulses d. **feedback path**	L1
11	Instability condition can be determined from a. table b. map c. graph d. **logic diagram**	L2
12	Transition table consists of a. **squares** b. rectangles c. circles d. oval	L2
13	A Condition occurs when an Asynchronous sequential circuit changes two or more binary states variables a. deadlock condition b. Running condition c. **Race condition** d. None	L4
14	Time delay device is the memory element of a. Unclocked flip-flops b. clocked flip-flops c. synchronous circuits d. **asynchronous circuits**	L5
15	The second step of making transition table is a. determining feedback loop b. **designating output of loops** c. deriving functions of Y d. plotting Y	L1
16	The NAND latch works when both inputs are a. **1** b. 0 c. inverted d. don't cares	L2
17	The effect of change in input more than one state is called a. undefined condition b. **race condition** c. reset condition	L2

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	d. ideal condition	
18	The change in state occurs during a. **pulse transition** b. outputs c. clock pulses d. inputs	L4
19	Asynchronous sequential logic circuit not uses a. inputs b. outputs c. **clock pulses** d. time	L5
20	Naming the states is done in a. transition table b. stable state c. **flow table** d. excitation table	L1
21	The delay elements provide a. large memory b. outputs c. clock pulses d. **short term memory**	L2
22	The analysis of Asynchronous sequential circuits are used to obtain a. **a table** b. a diagram c. graph d. both a and b	L2
23	Race condition is present in a. synchronous logic circuit b. **asynchronous logic circuit** c. ideal logic circuit d. both a and b	L4
24	During the design of asynchronous sequential circuits it is more convenient to name the state by letters this type of table called a. **Square table** b. Latch table c. Flow table d. None	L5
25	In the design procedure of asynchronous circuit, flow of table a. increased to maximum states b. **reduced to minimum states** c. changed d. remain same	L1

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26	The race in which stable state does not depends on order is called a . critical race b. identical race c. **non critical race** d. defined race	L2
27	The x variable in analysis procedure is used for a. rows b. **columns** c. matrix d. both a and b	L2
28	Asynchronous sequential logic circuits are used when primary need is a. time b. pressure c. **speed** d. accuracy	L4
29	Internal state and input values together are called a. full state b. **total state** c. initial state d. output state	L5
30	The change in state from 00 to 11 will cause change in a. **first variable** b. second variable c. third variable d. all variables	L1
31	The third step of making transition table is a. determining feedback loop b. designating output of loops c. **deriving functions of Y** d. plotting Y	L2
32	The y variable in analysis procedure is used for a. **rows** b. columns c. matrix d. both a and b	L2
33	The transition table gives values of a. 1's b. 0's c. x d. **y**	L4
34	Table having one state in each row is called a. transition table b. state table	L5

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	c. flow table d. **primitive flow table**	
35	The next states of asynchronous circuits are also called a. secondary variables b. primary variables c. **excitation variables** d. short term memory	L1
36	Memory elements in asynchronous circuits are a. **Unclocked flip-flops** b. clocked flip-flops c. clock pulses d. latches	L2
37	One of the properties of asynchronous circuits is a. identical mode b. map c. **feedback loop** d. chart	L2
38	Asynchronous sequential logic circuits usually perform operations in a. identical mode b. **fundamental mode** c. reserved mode d. reset mode	L4
39	In fundamental mode the circuit is assumed to be in a. unstable state b. **stable state** c. reset state d. clear state	L5
40	The circuit removing series of pulses is called a. defined circuit b. bounce circuit c. **DE-bounce circuit** d. undefined circuit	L1