

NADAR SARASWATHI COLLEGE OF ENGINEERING AND TECHNOLOGY, THENI.

Course/Branch : B.E/ECE	Year / Semester : IV/ VII	Format No.	NAC/TLP-07a.13
Subject Code : EC8791	Subject Name : Embedded and Real Time Systems	Rev. No.	02
Unit No : 2	Unit Name : ARM Processor and Peripherals	Date	30.09.2020

OBJECTIVE TYPE QUESTION BANK

S. No.	Objective Questions (MCQ /True or False / Fill up with Choices)	BTL
1	ARM stands for _____ a) Advanced Rate Machines b) Advanced RISC Machines c) Artificial Running Machines d) Aviary Running Machines	L2
2	The main importance of ARM micro-processors is providing operation with _____ a) Low cost and low power consumption b) Higher degree of multi-tasking c) Lower error or glitches d) Efficient memory management	L2
3	ARM processors where basically designed for _____ a) Main frame systems b) Distributed systems c) Mobile systems d) Super computers	L4
4	The ARM processors don't support Byte addressability. a) True b) False	L5
5	The address space in ARM is _____ a) 2^{24} b) 2^{64} c) 2^{16} d) 2^{32}	L1
6	The address system supported by ARM systems is/are _____ a) Little Endian b) Big Endian c) X-Little Endian d) Both Little & Big Endian	L1
7	Memory can be accessed in ARM systems by _____ instructions. i) Store ii) MOVE iii) Load iv) arithmetic	L2

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	v) logical a) i, ii, iii b) i, ii c) i, iv, v d) iii, iv, v	
8	RISC stands for _____ a) Restricted Instruction Sequencing Computer b) Restricted Instruction Sequential Compiler c) Reduced Instruction Set Computer d) Reduced Induction Set Computer	L1
9	In the ARM, PC is implemented using _____ a) Caches b) Heaps c) General purpose register d) Stack	L1
10	The additional duplicate register used in ARM machines are called as _____ a) Copied-registers b) Banked registers c) EXtra registers d) Extential registers	L3
11	The banked registers are used for _____ a) Switching between supervisor and interrupt mode b) Extended storing c) Same as other general purpose registers d) None of the mentioned	L2
12	Each instruction in ARM machines is encoded into _____ Word. a) 2 byte b) 3 byte c) 4 byte d) 8 byte	L3

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13	All instructions in ARM are conditionally executed. a) True b) False	L1
14	The addressing mode where the EA of the operand is the contents of Rn is _____ a) Pre-indexed mode b) Pre-indexed with write back mode c) Post-indexed mode d) None of the mentioned	L1
15	The effective address of the instruction written in Post-indexed mode, MOVE[Rn]+Rm is _____ a) EA = [Rn] b) EA = [Rn + Rm] c) EA = [Rn] + Rm d) EA = [Rm] + Rn	L2
16	PC 2148 pro development board has _____ on chip memory. a) 500k b) 625k c) 512k d) 425k	L3
17	In LPC 2148 we require separate programmer? a) True b) False	L1
18	Which LCD display is present in LPC 2148 Development Board? a) 8*8 LED b) 2*32 LCD c) 2*16 LCD connected peripherally d) 2*16 LCD on-chip	L5
19	Which IDE is supported by LPC2148 board? a) Code Blocks b) AVR Studio 4 c) Keil uVersion 4 d) Walldorf	L1
20	Timer in the board has _____ compare and _____ capture channels.	L1

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	a) 3 and 4 b) 4 and 3 c) 4 and 4 d) 3 and 3		
21	Finger print sensor uses which interface? a) USART protocol b) UART protocol c) SPI protocol d) I2C protocol		L2
22	UART is similar to _____ a) SPI protocol b) I2C protocol c) HTTP protocol d) MQTT protocol		L1
23	Communication in UART is _____ a) Only simple b) Only duplex c) Only full duplex d) Simplex, half duplex, full duplex		L1
24	What is WD1402A? a) SPI b) USART c) SPIUART d) I2C		L3
25	What is the speed of the 8250 UART? a) 4800bits/sec b) 1200bits/sec c) 12000bit/sec d) 9600bits/sec		L2
26	What is the processor used by ARM7? a) 8-bit CISC b) 8-bit RISC c) 32-bit CISC		L2

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	d) 32-bit RISC	
27	<p>What is the instruction set used by ARM7?</p> <p>a) 16-bit instruction set b) 32-bit instruction set c) 64-bit instruction set d) 8-bit instruction set</p>	L5
28	<p>What is the capability of ARM7 f instruction for a second?</p> <p>a) 110 MIPS b) 150 MIPS c) 125 MIPS d) 130 MIPS</p>	L2
29	<p>In Cortex-R processor series, which among the following represent/s dual core configuration along with the space saving the floating point unit?</p> <p>a. Cortex-R 4 b. Cortex-R 5 c. Cortex-R 7 d. All of the above</p>	L1
30	<p>In Cortex-A processor series, which among the following is the standalone and smallest processor in size constraints with high-end application support?</p> <p>a. Cortex-A5 b. Cortex-A9 c. Cortex-A53 d. Cortex-A59</p>	L1
31	<p>What are t, d, m, I stands for in ARM7TDMI?</p> <p>a) Timer, Debug, Multiplex, ICE b) Thumb, Debug, Multiplier, ICE c) Timer, Debug, Modulation, IS d) Thumb, Debug, Multiplier, ICE</p>	L2
32	<p>How many instructions pipelining is used in ARM7EJ-S?</p> <p>a) 3-Stage b) 4-Stage c) 5-Stage d) 2-stage</p>	L3

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33	In LPC 2148, which among the following is/are the functions of Mask register? a. Byte addressability b. Relocation to ARM local bus for fastest possible I/O timing c. Treating sets of port bits in the form of group without changing other bits d. All of the above	
34	Which mode of operation is exhibited by RS-485 standard? a. Single ended b. Differential c. Both a and b d. None of the above	
35	Which stage associated with pipelining mechanism recognizes the instruction that is to be executed? a. Fetch b. Decode c. Execute d. None of the above	

