Course/Branch : B.E / ECE	**Year / Semester** : III / V	Format No.	NAC/TLP-07a.13
Subject Code : EC8553	**Subject Name** : Discrete Time Signal Processing	Rev. No.	02
Unit No : 5	**Unit Name : Introduction to DSP**	Date	30.09.2020

OBJECTIVE TYPE QUESTION BANK

S. No.	Objective Questions (MCQ /True or False / Fill up with Choices)	BTL
1.	Program Sequence plays a crucial role in maintaining the track of _____ a. Program counter increment b. Conditional branching & looping c. Subroutine & interrupt handling d. All of the above ANSWER: D	L2
2.	In DSP Processor, what kind of queuing is undertaken/executed through instruction register and instruction cache? a. Implicate b. Explicate c. Both a and b d. None of the above answer: a	L2
3.	In TMS 320 C6x processor architecture, which functional unit is adopted for transferring the data from register to and from control register? a. L2 b. M2 c. S2 d. D2 answer: S2	L4
4.	**In TMS 320 C6x processor architecture, which operation/s is/are performed by 'M' functional unit?** **a.** Bit expansion **b.** Bit interleaving & deinterleaving **c.** Rotation & Variable shifting **d.** All of the above **ANSWER: All of the above**	L5

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5.	In C6X processor, which external device/s get/s acquire/s an interface support by EMIF peripheral? a. Synchronous burst b. Asynchronous devices c. Externally shared memory devices d. All of the above **ANSWER: All of the above**	L1
6.	Which peripheral on C 6 X processor allows buffering of serial samples in memory by port automatically & especially with an assistance of EDMA controller? a. Boot Loader b. HPI c. EMIF d. McBSP ANSWER: McBSP	L1
7.	Which address/es is/are generated by Program Sequences? a. Data Address b. Instruction Address c. Both a and b d. None of the above ANSWER: Instruction Address	L2
8.	In DAGs, which register/s provide/s increment or step size for index register especially during the register move? a. Index Register b. Length & Base Register	L1

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	c. Modify Register d. All of the above ANSWER: Modify Register	
9.	Which units are generally involved in Multiply and Accumulate (MAC)? a. Adder b. Multiplier c. Accumulator d. All of the above ANSWER: (d) All of the above	L1
10.	In DSP processors, which among the following maintains the track of addresses of input data as well as the coefficients stored in data and program memories? a. Data Address Generators (DAGs) b. Program sequences c. Barrel Shifter d. MAC ANSWER: (a) Data Address Generators (DAGs)	L3
11.	In TMS 320 C6x processor architecture, which operation/s is/are performed by 'M' functional unit? a. Bit expansion b. Bit interleaving & deinterleaving c. Rotation & Variable shifting d. All of the above ANSWER: All of the above	L2
12.	In DSP Processor, what kind of queuing is undertaken/executed through instruction register and instruction cache?	L3

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	a. Implicate b. Explicate c. Both a and b d. None of the above ANSWER: Implicate	
13.	Program Sequence plays a crucial role in maintaining the track of _____ a. Program counter increment b. Conditional branching & looping c. Subroutine & interrupt handling d. All of the above ANSWER: All of the above	L1
14.	Anti-imaging filter with cut-off frequency $\omega c = \pi / I$ is specifically used _____ upsampling process for the removal of unwanted images. a. Before b. At the time of c. After d. All of the above ANSWER: (c) After	L1
15.	How is the sampling rate conversion achieved by factor I/D? a. By increase in the sampling rate with (I) b. By filtering the sequence to remove unwanted images of spectra of original signal c. By decimation of filtered signal with factor D d. All of the above ANSWER: All of the above	L2
16.	In polyphase filters, the subfilters which share a common delay line results in the reduction of the	L3

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	storage requirement by factor _____ a. 1 b. 2 c. 3 d. 4 ANSWER: 3	
17.	Which type of programming is typically used for digital signal processors? [A]. Assembly language [B]. Machine language [C]. C [D]. None of the above Answer: Option A	L1
18.	Successive-approximation is perhaps the most widely used method of A/D conversion. A. True B. False Answer: Option A	L5
19.	An offset error in a DAC will show up as an incorrect analog output _____. A. only for higher value inputs B. only for lower value inputs C. only for certain (scattered) inputs D. for all inputs Answer: Option D	L1
20.	An ADC that compares each bit, one at a time, with the input analog signal is a _____. a single-slope ramp converter b dual-slope ramp converter c successive-approximation converter d tracking converter Answer: Option C	L1
21.	A standard logic device can be connected on a bus system as an open-collector logic device by connecting each output to a _____. a discrete transistor b 0 kΩ series resistor	L2

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	c light-emitting diode d CMOS buffer Answer: Option A	
22.	Which of the following rule is used in the bilinear transformation? a) Simpson's rule b) Backward difference c) Forward difference d) Trapezoidal rule Answer: d	L3
23.	Which of the following substitution is done in Bilinear transformations? a) s = 2T[1+z−11−z1] b) s = 2T[1+z−11+] c) s = 2T[1−z−11+z−1] d) None of the mentioned Answer: c	L1
24.	The total memory space of TMS 320C5x family of processes is a. 224 k words b. 224k bytes c. 192 k words d. 192 k bytes ANSWER: a	L5
25.	The size of data bus, A L U and accumulator in 320 c5x family of processors are respectively A. 16 bit 32 bit 40 bit B. 32 bit 32 bit 32 bit C. 16 bit 32 bit 32 bit D. 16 bit 40 bit 32 bit ANSWER: C	L1
26.	Which of the following is true with respect to axillary register arithmetic unit? a. it can be used for any other thematic operation b. it can be used for unsigned addition or subtraction c. it can be used for signed addition or subtraction d. it is used by the processor exclusively for address computations ANSWER: D	L1
27.	The architecture that employs instruction level parallelism is a. Von Neuman architecture b. Harvard architecture c. Modified Harvard architecture	L2

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	d. VLIW architecture ANSWER: d	
28.	The pipelining refers to a. Prefetching instructions and storing in a FIFO queue b. Fetching instruction and the data simultaneously c. Executing different phases of two or more instructions in parallel d. Executing different instruction in parallel using two or more computational units ANSWER: c	L3
29.	The number of programs and data buses in TMS320C54x processes are a. a two pairs of program buses and two pairs of data bases b. one pair of programmers and 3 pairs of date of bus c. 4 pairs of data or program bus d. 8 pairs of data or program bus ANSWER: a	L1
30.	The function of a wait state generator is a. to insert wait states in internal and external bus cycles b. to insert wait states in data memory cycles c. to insert wait states in program memory cycles d. to insert wait states in external bus cycles ANSWER: d	L2
31.	The upper 8 bits of 40 bit accumulator of TMS 320 c54x processor is called a. overflow bits b. sine extension bits c. Guard bits d. carry bits ANSWER: C	L2