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S. No.	Objective Questions (MCQ /True or False / Fill up with Choices)	BTL
1	Memory is a/an _____ a) Device to collect data from other computer b) Block of data to keep data separately **c) Indispensable part of computer** d) Device to connect through all over the world	L1
2	A flip flop stores _____ a) 10 bit of information **b) 1 bit of information** c) 2 bit of information d) 3-bit information	L2
3	A register is able to hold _____ a) Data **b) Word** c) Nibble d) Both data and word	L1
4	A register file holds _____ a) A large number of word of information b) A small number of word of information c) A large number of programs **d) A modest number of words of information**	L1
5	VLSI chip utilizes _____ a) NMOS b) CMOS c) BJT **d) All of the Mentioned**	L1
6	The full form of PLD is _____ a) Programmable Large Device b) Programmable Long Device **c) Programmable Logic Device** d) Programmable Lengthy Device	L1
7	ROM consist of _____ a) NOR and OR arrays b) NAND and NOR arrays **c) NAND and OR arrays** d) NOR and AND array	L1
8	The full form of EPROM is _____	L1

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	a) Easy Programmable Read Only Memory **b) Erasable Programmable Read Only Memory** c) Eradicate Programmable Read Only Memory d) Easy Programmable Read Out Memory	
9	ASIC stands for _____ a) Application Special Integrated Circuits b) Applied Special Integrated Circuits **c) Application Specific Integrated Circuits** d) Applied Specific Integrated Circuits	L1
10	The difference between FPGA and PLD is that _____ a) FPGA is slower than PLD b) FPGA has high power dissipation **c) FPGA incorporates logic blocks** d) All of the Mentioned	L2
11	Secondary memory is also known as _____ a) Registers b) Main Memory c) RAM **d) Both registers and main memory**	L2
12	Which of the following has the lowest access time? a) RAM b) ROM **c) Registers** d) Flag	L1
13	As the storage capacity of main memory is inadequate, which memory is used to enhance it? a) Secondary Memory b) Auxiliary Memory c) Static Memory **d) Both Secondary Memory and Auxiliary Memory**	L1
14	A sequential access memory is one in which _____ a) A particular memory location is accessed rapidly **b) A particular memory location is accessed sequentially** c) A particular memory location is accessed serially d) A particular memory location is accessed parallel	L2
15	A static memory is one in which _____ a) Content changes with time	L2

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	b) Content doesn't changes with time c) Memory is static always **d) Memory is dynamic always**	
16	A dynamic memory is one in which _____ a) Content changes with time b) Content doesn't changes with time c) Memory is static always **d) Memory is dynamic always**	L1
17	Dynamic memory cells use _____ as the storage device. a) The reactance of a transistor b) The impedance of a transistor **c) The capacitance of a transistor** d) The inductance of a transistor	L1
18	To store 1-bit of information, how many transistor is/are used _____ **a) 1** b) 2 c) 3 d) 4	L1
19	Static memory holds data as long as _____ a) AC power is applied **b) DC power is applied** c) Capacitor is fully charged d) High Conductivity	L1
20	Volatile memory refers to _____ a) The memory whose loosed data is achieved again when power to the memory circuit is removed **b) The memory which looses data when power to the memory circuit is removed** c) The memory which looses data when power to the memory circuit is applied d) The memory whose loosed data is achieved again when power to the memory circuit is applied	L2
21	Non-volatile memory refers to _____ **a) The memory whose loosed data is retained again when power to the memory circuit is removed/applied** b) The memory which looses data when power to the memory circuit is removed c) The memory which looses data when power to the memory circuit is applied d) The memory whose loosed data is achieved again when power to the memory circuit is applied	L2

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22	Which of the following has the capability to store the information permanently? a) RAM **b) ROM** c) Storage cells d) Both RAM and ROM	L2
23	ROM has the capability to perform _____ a) Write operation only **b) Read operation only** c) Both write and read operation d) Erase operation	L2
24	Since, ROM has the capability to read the information only then also it has been designed, why? a) For controlling purpose b) For loading purpose **c) For booting purpose** d) For erasing purpose	L2
25	Why are ROMs called non-volatile memory? a) They lose memory when power is removed **b) They do not lose memory when power is removed** c) They lose memory when power is supplied d) They do not lose memory when power is supplied	L2
26	The full form of EEPROM is _____ a) Erasable Electrically Programmable ROMs **b) Electrically Erasable Programmable ROMs** c) Electrically Erasable Programming ROMs d) Electrically Erasable Programmed ROMs	L1
27	Which of the following best describes EPROMs? a) EPROMs can be programmed only once **b) EPROMs can be erased by UV** c) EPROMs can be erased by shorting all inputs to the ground d) EPROMs can be erased electrically	L2
28	The Width of a processor's data path is measured in bits. Which of the following are common data paths? **a) 8 bits** b) 12 bits c) 16 bits d) 32 bits	L2
29	What is the major difference between DRAM and SRAM?	L2

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	a) Dynamic RAMs are always active; static RAMs must reset between data read/write cycles b) SRAMs can hold data via a static charge, even with power off c) The only difference is the terminal from which the data is removed—from the FET Drain or Source **d) DRAMs must be periodically refreshed**	
30	What does the term “random access” mean in terms of memory? a) Any address can be accessed in systematic order **b) Any address can be accessed in any order** c) Addresses must be accessed in a specific order d) Any address can be accessed in reverse order	L2
31	ROM may be programmed in _____ ways. **a) 2** b) 3 c) 4 d) 5	L1
32	Which programming is done during manufacturing process? **a) Mask Programming** b) PROM c) Both PROM and mask programming d) EPROM	L1
33	Which IC is a typical MSI/TTL based? **a) IC 74187** b) IC 74189 c) IC 74188 d) IC 74186	L2
34	The bit capacity of a memory that has 2048 addresses and can store 8 bits at each address is _____ a) 4096 **b) 16384** c) 32768 d) 8129	L2
35	How many 8 k × 1 RAMs are required to achieve a memory with a word capacity of 8 k and a word length of eight bits? **a) Eight** b) Two c) One d) Four	L3

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36	Which of the following best describes the fusible-link PROM? a) Manufacturer-programmable, reprogrammable b) Manufacturer-programmable, one-time programmable c) User-programmable, reprogrammable **d) User-programmable, one-time programmable**	L2
37	IC 74186 is of _____ a) 1024 bits b) 32 bits **c) 512 bits** d) 64 bits	L2
38	How many memory locations are addressed using 18 address bits? a) 165,667 b) 245,784 **c) 262,144** d) 212,342	L3
39	What is the bit storage capacity of a ROM with a 1024 × 8 organization? a) 1024 **b) 4096** c) 2048 d) 8192	L4
40	What is access time? a) The time taken to move a stored word from one bit to other bits after applying the address bits b) The time taken to write a word after applying the address bits **c) The time taken to read a stored word after applying the address bits** d) The time taken to erase a stored word after applying the address bits	L2
41	The chip by which both the operation of read and write is performed _____ **a) RAM** b) ROM c) PROM d) EPROM	L1
42	If a RAM chip has n address input lines then it can access memory locations upto _____ a) $2^{(n-1)}$ b) $2^{(n+1)}$ **c) 2^n** d) 2^{2n}	L2
43	The n-bit address is placed in the _____	L2

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	a) MBR **b) MAR** c) RAM d) ROM	
44	Computers invariably use RAM for _____ a) High complexity b) High resolution **c) High speed main memory** d) High flexibility	L2
45	Static RAM employs _____ a) BJT or MOSFET b) FET or JFET c) Capacitor or BJT **d) BJT or MOS**	L1
46	Dynamic RAM employs _____ **a) Capacitor or MOSFET** b) FET or JFET c) Capacitor or BJT d) BJT or MOS	L1
47	The memory capacity of a static RAM varies from _____ a) 32 bit to 64 bit b) 64 bit to 1024 bit **c) 64 bit to 1 Mega bit** d) 512 bit to 1 Mega bit	L3
48	The input data bit is written into the cell by setting _____ a) The flip-flop for 1 b) Resetting the flip-flop c) The flip-flop for HIGH **d) Both the flip-flop for 1 and resetting the flip-flop**	L4
49	Data is written in IC 7489 through _____ a) Chip select b) Enable **c) Data input** d) Memory enable	L2
50	What types of arrangements a TMS 4016 has? a) 1024 * 4 b) 1024 * 8	L4

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	c) 2048 * 4 **d) 2048 * 8**	
51	What is memory decoding? a) The process of Memory IC used in a digital system is overloaded with data **b) The process of Memory IC used in a digital system is selected for the range of address assigned** c) The process of Memory IC used in a digital system is selected for the range of data assigned d) The process of Memory IC used in a digital system is overloaded with data allocated in memory cell	L2
52	The first step in the design of memory decoder is _____ a) Selection of a EPROM b) Selection of a RAM **c) Address assignment** d) Data insertion	L2
53	How many address bits are required to select memory location in Memory decoder? a) 4 KB b) 8 KB **c) 12 KB** d) 16 KB	L4
54	IC 4116 is organised as _____ a) 512 * 4 b) 16 * 1 **c) 32 * 4** d) 64 * 2	L5
55	To construct 16K * 4-bit memory, how many 4116 ICs are required? a) 1 b) 2 c) 3 **d) 4**	L6
56	How many 1024 * 1 RAM chips are required to construct a 1024 * 8 memory system? a) 4 b) 6 **c) 8** d) 12	L6
57	How many 16K * 4 RAMs are required to achieve a memory with a capacity of	L5

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	64K and a word length of 8 bits? a) 2 b) 4 c) 6 **d) 8**	
58	The full form of PLD is _____ a) Programmable Load Devices b) Programmable Logic Data **c) Programmable Logic Devices** d) Programmable Loaded Devices	L2
59	PLD contains a large number of _____ a) Flip-flops b) Gates c) Registers **d) All of the Mentioned**	L2
60	In PLD, there are provisions to perform interconnections of the gates internally, because of _____ a) High reliability b) High conductivity **c) The desired logic implementation** d) The desired output	L1
61	Why antifuses are implemented in a PLD? a) To protect from high voltage b) To increase the memory **c) To implement the programmes** d) As a switching devices	L1
62	PLA refers to _____ a) Programmable Loaded Array b) Programmable Array Logic **c) Programmable Logic Array** d) Programmed Array Logic	L1
63	The inputs in the PLD is given through _____ a) NAND gates b) OR gates c) NOR gates	L2

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	d) AND gates	
64	Outputs of the AND gate in PLD is known as _____ a) Input lines **b) Output lines** c) Strobe lines d) Control lines	L1
65	PLA contains _____ **a) AND and OR arrays** b) NAND and OR arrays c) NOT and AND arrays d) NOR and OR arrays	L1
66	PLA is used to implement _____ a) A complex sequential circuit b) A simple sequential circuit **c) A complex combinational circuit** d) A simple combinational circuit	L2
67	A PLA is similar to a ROM in concept except that _____ a) It hasn't capability to read only b) It hasn't capability to read or write operation **c) It doesn't provide full decoding to the variables** d) It hasn't capability to write only	L2
68	The complex programmable logic device contains several PLD blocks and _____ a) A language compiler b) AND/OR arrays c) Global interconnection matrix **d) Field-programmable switches**	L2
69	Which type of device FPGA are? a) SLD b) SROM c) EPROM **d) PLD**	L2
70	The difference between a PAL & a PLA is _____ a) PALs and PLAs are the same thing **b) The PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane** c) The PAL has a programmable OR plane and a programmable AND plane, while the PLA only has a programmable AND plane	L2

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	d) The PAL has more possible product terms than the PLA	
71	If a PAL has been programmed once _____ a) Its logic capacity is lost b) Its outputs are only active HIGH c) Its outputs are only active LOW **d) It cannot be reprogrammed**	L2
72	Applications of PLAs are _____ a) Registered PALs b) Configurable PALs c) PAL programming **d) All of the Mentioned**	L1
73	In RTL NOR gate, the output is at logic 1 only when all the inputs are at _____ **a) logic 0** b) logic 1 c) +10V d) Floating	L1
74	Resistor–transistor logic (RTL) is a class of digital circuits built using _____ as the input network and _____ as switching devices. **a) Resistors, bipolar junction transistors (BJTs)** b) Bipolar junction transistors (BJTs), Resistors c) Capacitors, resistors d) Resistors, capacitors	L2
75	RTL consists of a common emitter stage with a _____ connected between the base and the input voltage source. a) collector **b) base resistor** c) capacitor d) inductor	L2
76	The role of the _____ is to convert the collector current into a voltage in RTL. **a) Collector resistor** b) Base resistor c) Capacitor d) Inductor	L2
77	TTL circuits with “totem-pole” output stage minimize _____ **a) The power dissipation in RTL** b) The time consumption in RTL c) The speed of transferring rate in RTL	L2

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	d) Propagation delay in RTL	
78	The minimum number of transistors can be used by 2 input AND gate is _____ **a) 2** b) 3 c) 4 d) 5	L1
79	In DTL logic gating function is performed by _____ **a) Diode** b) Transistor c) Inductor d) Capacitor	L1
80	In DTL amplifying function is performed by _____ a) Diode **b) Transistor** c) Inductor d) Capacitor	L1
81	How many stages a DTL consist of? a) 2 **b) 3** c) 4 d) 5	L1
82	The way to speed up DTL is to add an across intermediate resister is _____ **a) Small "speed-up" capacitor** b) Large "speed-up" capacitor c) Small "speed-up" transistor d) Large " speed-up" transistor	L1
83	To increase fan-out of the gate in DTL _____ a) An additional capacitor may be used b) An additional resister may be used **c) An additional transistor and diode may be used** d) Only an additional diode may be used	L1
84	Transistor–transistor logic (TTL) is a class of digital circuits built from _____ a) JFET only b) Bipolar junction transistors (BJT) c) Resistors	L1

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	d) Bipolar junction transistors (BJT) and resistors	
85	TTL is called transistor–transistor logic because both the logic gating function and the amplifying function are performed by _____ a) Resistors **b) Bipolar junction transistors** c) One transistor d) Resistors and transistors respectively	L2
86	TTL inputs are the emitters of a _____ a) Transistor-transistor logic **b) Multiple-emitter transistor** c) Resistor-transistor logic d) Diode-transistor logic	L2
87	TTL is a _____ **a) Current sinking** b) Current sourcing c) Voltage sinking d) Voltage sourcing	L2
88	The speed of _____ circuits is limited by the tendency of common emitter circuits to go into saturation. **a) TTL** b) ECL c) RTL d) DTL	L2
89	The full form of ECL is _____ a) Emitter-collector logic b) Emitter-complementary logic **c) Emitter-coupled logic** d) Emitter-cored logic	L1
90	In an ECL the output is taken from _____ a) Emitter b) Base **c) Collector** d) Junction of emitter and base	L1
91	The ECL behaves as _____ a) NOT gate **b) NOR gate** c) NAND gate d) AND gate	L1

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92	The ECL circuits usually operates with _____ **a) Negative voltage** b) Positive voltage c) Grounded voltage d) High Voltage	L1
93	CMOS technology is used in _____ a) Inverter b) Microprocessor c) Digital logic **d) Both microprocessor and digital logic**	L1
94	Two important characteristics of CMOS devices are _____ a) High noise immunity b) Low static power consumption c) High resistivity **d) Both high noise immunity and low static power consumption**	L2
95	CMOS behaves as a/an _____ a) Adder b) Subtractor **c) Inverter** d) Comparator	L1
96	An important characteristic of a CMOS circuit is the _____ a) Noise immunity **b) Duality** c) Symmetricity d) Noise Margin	L1
97	CMOS logic dissipates _____ power than NMOS logic circuits. a) More **b) Less** c) Equal d) Very High	L1