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Subject Code : EE8351	**Subject Name** : DIGITAL LOGIC CIRCUITS	Rev. No.	02
Unit No : 1	**Unit Name : NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES**	Date	30.09.2020

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S. No.	Objective Questions (MCQ /True or False / Fill up with Choices)	BTL
1	Any signed negative binary number is recognised by its _____ **a) MSB** b) LSB c) Byte d) Nibble	L1
2	The parameter through which 16 distinct values can be represented is known as _____ a) Bit b) Byte **c) Word** d) Nibble	L1
3	If the decimal number is a fraction then its binary equivalent is obtained by _____ the number continuously by 2. a) Dividing **b) Multiplying** c) Adding d) Subtracting	L2
4	The representation of octal number (532.2)8 in decimal is _____ **a) $(346.25)_{10}$** b) $(532.864)_{10}$ c) $(340.67)_{10}$ d) $(531.668)_{10}$	L3
5	The decimal equivalent of the binary number (1011.011)2 is _____ **a) (11.375)10** b) (10.123)10 c) (11.175)10 d) (9.23)10	L3
6	An important drawback of binary system is _____ **a) It requires very large string of 1's and 0's to represent a decimal number** b) It requires sparingly small string of 1's and 0's to represent a decimal number c) It requires large string of 1's and small string of 0's to represent a decimal number d) It requires small string of 1's and large string of 0's to represent a decimal number	L2

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7	The decimal equivalent of the octal number $(645)_8$ is _____ a) $(450)_{10}$ b) $(451)_{10}$ **c) $(421)_{10}$** d) $(501)_{10}$	L4
8	The largest two digit hexadecimal number is _____ a) (FE)16 b) (FD)16 **c) (FF)16** d) (EF)16	L3
9	Representation of hexadecimal number (6DE)H in decimal: **a) $6 * 16^2 + 13 * 16^1 + 14 * 16^0$** b) $6 * 16^2 + 12 * 16^1 + 13 * 16^0$ c) $6 * 16^2 + 11 * 16^1 + 14 * 16^0$ d) $6 * 16^2 + 14 * 16^1 + 15 * 16^0$	L5
10	The given hexadecimal number (1E.53)16 is equivalent to _____ a) (35.684)8 **b) (36.246)8** c) (34.340)8 d) (35.599)8	L3
11	The octal number (651.124)8 is equivalent to _____ **a) (1A9.2A)16** b) (1B0.10)16 c) (1A8.A3)16 d) (1B0.B0)16	L5
23	The octal equivalent of the decimal number (417)10 is _____ **a) (641)8** b) (619)8 c) (640)8 d) (598)8	L5
13	Convert the hexadecimal number (1E2)16 to decimal: a) 480 b) 483 **c) 482** d) 484	L3
14	(170)10 is equivalent to a) (FD)16 b) (DF)16 **c) (AA)16** d) (AF)16	L3
15	Convert (214)8 into decimal: **a) (140)10**	L5

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	b) (141)10 c) (142)10 d) (130)10	
16	Convert (0.345)10 into an octal number: a) (0.16050)8 **b) (0.26050)8** c) (0.19450)8 d) (0.24040)8	L5
17	Convert the binary number (01011.1011)2 into decimal: **a) (11.6875)10** b) (11.5874)10 c) (10.9876)10 d) (10.7893)10	L3
18	Octal to binary conversion: (24)8 =? a) (111101)2 **b) (010100)2** c) (111100)2 d) (101010)2	L3
19	Convert binary to octal: (110110001010)2 =? a) (5512)8 **b) (6612)8** c) (4532)8 d) (6745)8	L3
20	Binary coded decimal is a combination of _____ a) Two binary digits b) Three binary digits **c) Four binary digits** d) Five binary digits	L3
21	The decimal number 10 is represented in its BCD form as _____ a) 10100000 b) 01010111 **c) 00010000** d) 00101011	L2
22	Add the two BCD numbers: 1001 + 0100 = ? a) 10101111 b) 01010000 **c) 00010011** d) 00101011	L3
23	Carry out BCD subtraction for (68) – (61) using 10's complement method. **a) 00000111** b) 01110000 c) 100000111 d) 011111000	L3
24	Code is a symbolic representation of _____ information. a) Continuous	L2

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	b) Discrete c) Analog d) Both continuous and discrete	
25	A three digit decimal number requires _____ for representation in the conventional BCD format. a) 3 bits b) 6 bits **c) 12 bits** d) 24 bits	L3
25	How many bits would be required to encode decimal numbers 0 to 9999 in straight binary codes? a) 12 b) 14 **c) 16** d) 18	L3
26	The excess-3 code for 597 is given by _____ **a) 100011001010** b) 100010100111 c) 010110010111 d) 010110101101	L3
27	The decimal equivalent of the excess-3 number 110010100011.01110101 is _____ **a) 970.42** b) 1253.75 c) 861.75 d) 1132.87	L3
28	In boolean algebra, the OR operation is performed by which properties? a) Associative properties b) Commutative properties c) Distributive properties **d) All of the Mentioned**	L2
29	The expression for Absorption law is given by _____ **a) A + AB = A** b) A + AB = B c) AB + AA' = A d) A + B = B + A	L2
30	According to boolean law: A + 1 = ? **a) 1** b) A c) 0 d) A'	L3
31	The involution of A is equal to _____ **a) A** b) A' c) 1	L2

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	d) 0	
32	A(A + B) = ? a) AB b) 1 c) (1 + AB) **d) A**	L2
33	DeMorgan's theorem states that _____ **a) (AB)' = A' + B'** b) (A + B)' = A' * B c) A' + B' = A'B' d) (AB)' = A' + B	L2
34	(A + B)(A' * B') = ? a) 1 **b) 0** c) AB d) AB'	L3
35	Complement of the expression A'B + CD' is _____ a) (A' + B)(C' + D) b) (A + B')(C' + D) c) (A' + B)(C' + D) d) (A + B')(C + D')	L5
36	Simplify Y = AB' + (A' + B)C. **a) AB' + C** b) AB + AC c) A'B + AC' d) AB + A	L5
37	The boolean function A + BC is a reduced form of _____ a) AB + BC **b) (A + B)(A + C)** c) A'B + AB'C d) (A + C)B	L4
38	All input of NOR as low produces result as _____ a) Low b) Mid **c) High** d) Floating	L2
39	In RTL NOR gate, the output is at logic 1 only when all the inputs are at _____ **a) logic 0** b) logic 1 c) +10V d) Floating	L1
40	Resistor–transistor logic (RTL) is a class of digital circuits built using _____ as the input network and _____ as switching devices. **a) Resistors, bipolar junction transistors (BJTs)**	L2

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	b) Bipolar junction transistors (BJTs), Resistors c) Capacitors, resistors d) Resistors, capacitors	
41	RTL consists of a common emitter stage with a _____ connected between the base and the input voltage source. a) collector **b) base resistor** c) capacitor d) inductor	L2
42	The role of the _____ is to convert the collector current into a voltage in RTL. **a) Collector resistor** b) Base resistor c) Capacitor d) Inductor	L2
43	TTL circuits with “totem-pole” output stage minimize _____ **a) The power dissipation in RTL** b) The time consumption in RTL c) The speed of transferring rate in RTL d) Propagation delay in RTL	L2
44	The minimum number of transistors can be used by 2 input AND gate is _____ **a) 2** b) 3 c) 4 d) 5	L1
45	In DTL logic gating function is performed by _____ **a) Diode** b) Transistor c) Inductor d) Capacitor	L1
46	In DTL amplifying function is performed by _____ a) Diode **b) Transistor** c) Inductor d) Capacitor	L1
47	How many stages a DTL consist of? a) 2 **b) 3** c) 4 d) 5	L1
48	The way to speed up DTL is to add an across intermediate resister is _____ **a) Small “speed-up” capacitor** b) Large “speed-up” capacitor c) Small “speed-up” transistor	L1

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	d) Large ” speed-up” transistor	
49	To increase fan-out of the gate in DTL _____ a) An additional capacitor may be used b) An additional resister may be used **c) An additional transistor and diode may be used** d) Only an additional diode may be used	L1
50		L2
51	Transistor–transistor logic (TTL) is a class of digital circuits built from _____ a) JFET only b) Bipolar junction transistors (BJT) c) Resistors **d) Bipolar junction transistors (BJT) and resistors**	
52	TTL is called transistor–transistor logic because both the logic gating function and the amplifying function are performed by _____ a) Resistors **b) Bipolar junction transistors** c) One transistor d) Resistors and transistors respectively	L2
53	TTL inputs are the emitters of a _____ a) Transistor-transistor logic **b) Multiple-emitter transistor** c) Resistor-transistor logic d) Diode-transistor logic	L2
54	TTL is a _____ **a) Current sinking** b) Current sourcing c) Voltage sinking d) Voltage sourcing	L2
55	The speed of _____ circuits is limited by the tendency of common emitter circuits to go into saturation. **a) TTL** b) ECL c) RTL d) DTL	L2
56	The full form of ECL is _____ a) Emitter-collector logic b) Emitter-complementary logic **c) Emitter-coupled logic** d) Emitter-cored logic	L1
57	In an ECL the output is taken from _____ a) Emitter b) Base	L1

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	c) Collector d) Junction of emitter and base	
58	The ECL behaves as _____ a) NOT gate **b) NOR gate** c) NAND gate d) AND gate	L1
59	The ECL circuits usually operates with _____ **a) Negative voltage** b) Positive voltage c) Grounded voltage d) High Voltage	L1
60	CMOS technology is used in _____ a) Inverter b) Microprocessor c) Digital logic **d) Both microprocessor and digital logic**	L1
61	Two important characteristics of CMOS devices are _____ a) High noise immunity b) Low static power consumption c) High resistivity **d) Both high noise immunity and low static power consumption**	L2
62	CMOS behaves as a/an _____ a) Adder b) Subtractor **c) Inverter** d) Comparator	L1
63	An important characteristic of a CMOS circuit is the _____ a) Noise immunity **b) Duality** c) Symmetricity d) Noise Margin	L1
64	CMOS logic dissipates _____ power than NMOS logic circuits. a) More **b) Less** c) Equal d) Very High	L1
65	Semiconductors are made of _____ **a) Ge and Si** b) Si and Pb c) Ge and Pb d) Pb and Au	L1
66	How many outputs are present in a BCD decoder? a) 4 b) 5	L2

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	c) 15 **d) 10**	
67	What control signals may be necessary to operate a 1-line-to-16 line decoder? a) Flasher circuit control signal **b) A LOW on all gate enable inputs** c) Input from a hexadecimal counter d) A HIGH on all gate enable circuits	L3
68	How many inputs are required for a 1-of-10 BCD decoder? **a) 4** b) 8 c) 10 d) 2	L4
69	Which error detection method uses one's complement arithmetic? a) Simple parity check b) Two-dimensional parity check c) CRC **d) Checksum**	L3
70	Which error detection method consists of just one redundant bit per data unit? **a) Simple parity check** b) Two-dimensional parity check c) CRC d) Checksum	L2
71	What is a parity bit? **a) An error detection is achieved by adding an extra bit** b) After addition, the carry is found c) Bit generated during data transmission d) After addition, the total number of bits	L2
72	The BCD number 101011 has _____ priority. **a) Even** b) Odd c) Both even and odd d) Undefined	L3
73	Which error detection method involves polynomials? a) Simple parity check **b) CRC** c) Two-dimensional parity check d) Checksum	L2
74	The odd parity output of decimal number 9 is _____ a) 0 **b) 1** c) 1001 d) 0011	L2
75	If odd parity is used for ASCII error detection, the number of 0s per 8-bit symbol is _____	L2

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	a) Indeterminate b) 42 c) Even d) Odd	