Course/Branch : BE/ EEE	**Year / Semester** : III / V	Format No.	NAC/TLP-07a.13
Subject Code :EE8551	**Subject Name** :Microprocessors and Microcontrollers	Rev. No.	02
Unit No : 02	**Unit Name** : Programming Of 8085 Processor	Date	30.09.2020

OBJECTIVE TYPE QUESTION BANK

S. No.	Objective Questions (MCQ /True or False / Fill up with Choices)	BTL
1	How many types of basic multiprocessor configurations? A) 2 B) 3 **C) 4** D) 5	L1
2	A _____ is a specially designed circuit on microprocessor chip which can perform the same task very quickly, which the microprocessor performs A) Coprocessor configuration B) Closely coupled configuration C) Loosely coupled configuration **D) None of the above**	L2
3	The coprocessor and the processor is connected via? **A) TEST** B) QS0 C) QS1 D) All of the above	L1
4	It is a power supply signal, which requires +5V supply for the operation of the circuit. A) VCA B) VDD **C) VCC** D) INTA.	L2
5	The _____ handles all the communication between the processor and the memory A) numeric extension unit B) Packed Unit **C) control unit** D) Binary Unit	L3
6	In 8085 microprocessor system with memory mapped I/O, which of the following is true? A) Devices have 8-bit address line B) Devices are accessed using IN and OUT instructions	L2

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	C) There can be maximum of 256 input devices and 256 output devices **D) Arithmetic and logic operations can be directly performed with the I/O data**	
7	An interrupt breaks the execution of instructions and diverts its execution to **A) Interrupt service routine** B) Counter word register C) Execution unit D) control unit	L1
8	While executing the main program, if two or more interrupts occur, then the sequence of appearance of interrupts is called A) multi-interrupt B) nested interrupt C) interrupt within interrupt **D) nested interrupt and interrupt within interrupt**	L2
9	NMI stands for **A) nonmaskable interrupt** B) nonmultiple interrupt C) nonmovable interrupt D) none of the mentioned	L1
10	If any interrupt request given to an input pin cannot be disabled by any means then the input pin is called A) maskable interrupt **B) nonmaskable interrupt** C) maskable interrupt and nonmaskable interrupt D) none of the mentioned	L2
11	The INTR interrupt may be **A) maskable** B) nonmaskable C) maskable and nonmaskable D) none of the mentioned	L1
12	While CPU is executing a program, an interrupt exists then it	L2

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	A) follows the next instruction in the program B) jumps to instruction in other registers **C) breaks the normal sequence of execution of instructions** D) stops executing the program	
13	Whenever a number of devices interrupt a CPU at a time, and if the processor is able to handle them properly, it is said to have A) interrupt handling ability B) interrupt processing ability **C) multiple interrupt processing ability** D) multiple interrupt executing ability	L2
14	The Programmable interrupt controller is required to **A) handle one interrupt request** B) handle one or more interrupt requests at a time C) handle one or more interrupt requests with a delay D) handle no interrupt request	L1
15	The INTR interrupt may be masked using the flag A) direction flag B) overflow flag **C) interrupt flag** D) sign flag	L2
16	In 8085 microprocessor how many interrupts are maskable A) Two B) Three **C) Four** D) Five	L1
17	Which stack is used in 8085 microprocessor A) FIFO B) FILO **C) LIFO** D) LILO	L1

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18	In this instruction of the 8085 microprocessor how many bytes are present A) One or two **B) One , two or three** C) One only D) Two or Three	L2
19	Which one of the following addressing technique is not used in 8085 microprocessor A) Register B) Immediate C) Register indirect **D) Relative**	L1
20	Which one of the following register of 8085 microprocessor is not a part of the programming model A) Instruction register B) Memory address register **C) Status register** D) Temporary data register	L1
21	The program counter in 8085 microprocessor is a 16 bit register because A) It counts 16 bits at a time **B) There are 16 address times** C) It facilitates the users storing 16 bit data temporarily D) It has to fetch two 8 bit data at a time	L2
22	A direct memory access (DMA) transfer replies A) Direct transfer of data between memory and accumulator **B) Direct transfer of data between memory and I/O devices without the use of microprocessor** C) Transfer of data exclusively within microprocessor registers D) A fast transfer of data between microprocessor and I/O devices	L1
23	Handshaking mode of data transfer is **A) Synchronous data transfer** B) asynchronous data transfer C) interrupt driven data transfer	L1

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	D) level mode of DMA data transfer	
24	In a microprocessor the address of the new next instruction to be executed is stored in A) Stack pointer **B)** Address latch **C) Program counter** D) General purpose register	L2
25	The instruction RET executes with the following series of machine cycle A) Fetch, read, write **B) Fetch, write, write** C) Fetch, read, read D) Fetch, read	L2
26	Which one of the following statements is correct regarding the instruction CMP A **A) Compare accumulator with register A** B) Compare accumulator with memory C) Compare accumulator with register H D) Instruction does not exist	L1
27	The instruction JNC 16 – bit refers to jump to 16 – bit address if A) Sign flag is set **B) Carry flag is reset** C) Zero flag is set D) Parity flag is reset	L1
28	Among the given instructions, the which affects the maximum number of flags is A) RAL B) POP PSW **C) XRA A** D) DCR A	L1
29	XCHG instruction of 8085 exchange the content of A) Top of stack with contents of register pair B) BC and DE register pairs	L1

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	C) HL and DE register pairs D) None of the above	
30	Direction flag is used with **A) String instructions** B) Stack instructions C) Arithmetic instructions D) Branch instructions	L2
31	Following is a 16 bit register for 8085 microprocessor A) Stack pointer **B) Accumulator** C) Register B D) Register C	L1
32	The register inform which holds the information about the nature of results of arithmetic of logic operations is called as A) Accumulator B) Condition code register **C) Flag register** D) Process status registers	L1
33	When referring to instruction words a mnemonic is A) A short abbreviation for the operand address **B) A short abbreviation for the operation to be performed** C) A short abbreviation for the data word stored at the operand address D) Shorthand for machine language	L1
34	A microprocessor retries instructions from : A) Control memory B) Cache memory **C) Main memory** D) Virtual memory	L2
35	How many bits the instruction pointer is wide: **A) 16 bit** B) 32 bit	L1

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	C) 64 bit D) 128 bit	
36	A machine language instructions format consists of A) Operation code field. **B) Operation code field & operand field** C) Operand field D) none of the mentioned	L1
37	IP Stand for: **A) Instruction pointer** B) Instruction purpose C) Instruction paints D) None of these	L2
38	The instruction MOVAX, 123H is an example of A) register addressing mode **B) immediate addressing mode** C) based indexed addressing mode D) direct addressing mode	L1
39	Which of the following is true about Control and status signals? A) These signals are used to identify the nature of operation. B) There are 3 control signal and 3 status signals. C) Three status signals are IO/M, S0 & S1. **D) All of the above**	L1
40	How many and what are the machine cycles needed foe execution of PUSH B? A) 2, 1 Fetch and 1 Memory write **B) 3, 1 Fetch and 2 Memory write** C) 3, 1 Fetch , 1 Memory read and 1 Memory write D) 3, 1 Fetch and 2 Memory read	L2