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Subject Code : EE8351	**Subject Name** : DIGITAL LOGIC CIRCUITS	Rev. No.	02
Unit No : 2	**Unit Name : COMBINATIONAL CIRCUITS**	Date	30.09.2020

OBJECTIVE TYPE QUESTION BANK

S. No.	Objective Questions (MCQ /True or False / Fill up with Choices)	BTL
1	The logical sum of two or more logical product terms is called _____ **a) SOP** b) POS c) OR operation d) NAND operation	L1
2	The expression Y=AB+BC+AC shows the _____ operation. a) EX-OR **b) SOP** c) POS d) NOR	L3
3	The expression Y=(A+B)(B+C)(C+A) shows the _____ operation. a) AND **b) POS** c) SOP d) NAND	L3
4	A product term containing all K variables of the function in either complemented or uncomplemented form is called a _____ **a) Minterm** b) Maxterm c) Midterm d) ∑ term	L2
5	According to the property of minterm, how many combination will have value equal to 1 for K input variables? a) 0 **b) 1** c) 2 d) 3	L3
6	The canonical sum of product form of the function y(A,B) = A + B is _____ a) AB + BB + A'A **b) AB + AB' + A'B** c) BA + BA' + A'B' d) AB' + A'B + A'B'	L4
7	Maxterm is the sum of _____ of the corresponding Minterm with its literal complemented. **a) Terms** b) Words c) Numbers	L2

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	d) Nibble	
8	Canonical form is a unique way of representing _____ a) SOP b) Minterm **c) Boolean Expressions** d) POS	L2
9	_____ expressions can be implemented using either (1) 2-level AND-OR logic circuits or (2) 2-level NAND logic circuits. a) POS b) Literals **c) SOP** d) POS	L3
10	A Karnaugh map (K-map) is an abstract form of _____ diagram organized as a matrix of squares. **a) Venn Diagram** b) Cycle Diagram c) Block diagram d) Triangular Diagram	L2
11	There are _____ cells in a 4-variable K-map. a) 12 **b) 16** c) 18 d) 8	L2
23	The K-map based Boolean reduction is based on the following Unifying Theorem: A + A' = 1. a) Impact **b) Non Impact** c) Force d) Complementarity	L2
13	Each product term of a group, w'.x.y' and w.y, represents the _____in that group. a) Input b) POS **c) Sum-of-Minterms** d) Sum of Maxterms	L2
14	The prime implicant which has at least one element that is not present in any other implicant is known as _____ **a) Essential Prime Implicant** b) Implicant c) Complement d) Prime Complement	L2
15	Product-of-Sums expressions can be implemented using _____ a) 2-level OR-AND logic circuits b) 2-level NOR logic circuits c) 2-level XOR logic circuits **d) Both 2-level OR-AND and NOR logic circuits**	L3

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16	Each group of adjacent Minterms (group size in powers of twos) corresponds to a possible product term of the given _____ **a) Function** b) Value c) Set d) Word	L2
17	Don't care conditions can be used for simplifying Boolean expressions in _____ a) Registers b) Terms **c) K-maps** d) Latches	L2
18	It should be kept in mind that don't care terms should be used along with the terms that are present in _____ **a) Minterms** b) Expressions c) K-Map d) Latches	L2
19	Using the transformation method you can realize any POS realization of OR-AND with only. a) XOR b) NAND c) AND **d) NOR**	L3
20	There are many situations in logic design in which simplification of logic expression is possible in terms of XOR and _____ operations. **a) X-NOR** b) XOR c) NOR d) NAND	L4
21	The code where all successive numbers differ from their preceding number by single bit is _____ a) Alphanumeric Code b) BCD c) Excess 3 **d) Gray**	L3
22	The following switching functions are to be implemented using a decoder: f1 = ∑m(1, 2, 4, 8, 10, 14) f2 = ∑m(2, 5, 9, 11) f3 = ∑m(2, 4, 5, 6, 7) The minimum configuration of decoder will be _____ a) 2 to 4 line b) 3 to 8 line **c) 4 to 16 line** d) 5 to 32 line	L5
23	How many AND gates are required to realize Y = CD + EF + G? a) 4 b) 5	L6

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	c) 3 **d) 2**	
24	The NOR gate output will be high if the two inputs are _____ **a) 00** b) 01 c) 10 d) 11	L2
25	How many two-input AND and OR gates are required to realize Y = CD+EF+G? **a) 2, 2** b) 2, 3 c) 3, 3 d) 3, 2	L6
25	A universal logic gate is one which can be used to generate any logic function. Which of the following is a universal logic gate? a) OR b) AND c) XOR **d) NAND**	L5
26	A full adder logic circuit will have _____ a) Two inputs and one output b) Three inputs and three outputs c) Two inputs and two outputs **d) Three inputs and two outputs**	L4
27	Which of following are known as universal gates? **a) NAND & NOR** b) AND & OR c) XOR & OR d) EX-NOR & XOR	L2
28	The gates required to build a half adder are _____ a) EX-OR gate and NOR gate b) EX-OR gate and OR gate **c) EX-OR gate and AND gate** d) EX-NOR gate and AND gate	L2
29	A single transistor can be used to build which of the following digital logic gates? a) AND gates b) OR gates **c) NOT gates** d) NAND gates	L2
30	How many truth table entries are necessary for a four-input circuit? a) 4 b) 8 c) 12 **d) 16**	L3
31	Exclusive-OR (XOR) logic gates can be constructed from what other logic gates? a) OR gates only b) AND gates and NOT gates	L3

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	c) AND gates, OR gates, and NOT gates d) OR gates and NOT gates	
32	The basic logic gate whose output is the complement of the input is the _____ a) OR gate b) AND gate **c) INVERTER gate** d) XOR gate	L2
33	The AND function can be used to _____ and the OR function can be used to _____ **a) Enable, disable** b) Disable, enable c) Synchronize, energize d) Detect, invert	L2
34	It is possible for an enable or strobe input to undergo an expansion of two or more MUX ICs to the digital multiplexer with the proficiency of large number of _____ **a) Inputs** b) Outputs c) Selection lines d) Enable lines	L2
35	One multiplexer can take the place of _____ a) Several SSI logic gates b) Combinational logic circuits c) Several Ex-NOR gates **d) Several SSI logic gates or combinational logic circuits**	L2
36	If the number of n selected input lines is equal to 2^m then it requires _____ select lines. a) 2 **b) m** c) n d) 2^n	L3
37	How many select lines would be required for an 8-line-to-1-line multiplexer? a) 2 b) 4 c) 8 **d) 3**	L2
38	The enable input is also known as _____ a) Select input b) Decoded input **c) Strobe** d) Sink	L1
39	4 to 1 MUX would have _____ a) 2 inputs b) 3 inputs **c) 4 inputs**	L2

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	d) 5 inputs	
40	The two input MUX would have _____ **a) 1 select line** b) 2 select lines c) 4 select lines d) 3 select lines	L2
41	A combinational circuit is one in which the output depends on the _____ **a) Input combination at the time** b) Input combination and the previous output c) Input combination at that time and the previous input combination d) Present output and the previous output	L3
42	Without any additional circuitry an 8:1 MUX can be used to obtain _____ a) Some but not all Boolean functions of 3 variables b) All function of 3 variables but none of 4 variables c) All functions of 3 variables and some but not all of 4 variables **d) All functions of 4 variables**	L2
43	One multiplexer can take the place of _____ a) Several SSI logic gates b) Combinational logic circuits c) Several Ex-NOR gates **d) Several SSI logic gates or combinational logic circuits**	L3
44	Why is a demultiplexer called a data distributor? **a) The input will be distributed to one of the outputs** b) One of the inputs will be selected for the output c) The output will be distributed to one of the inputs d) Single input to Single Output	L4
45	Most demultiplexers facilitate which type of conversion? a) Decimal-to-hexadecimal **b) Single input, multiple outputs** c) AC to DC d) Odd parity to even parity	L3
46	In 1-to-4 multiplexer, if C1 = 0 & C2 = 1, then the output will be _____ a) Y0 **b) Y1** c) Y2 d) Y3	L4
47	How many select lines are required for a 1-to-8 demultiplexer? a) 2 **b) 3** c) 4 d) 5	L4
48	How many AND gates are required for a 1-to-8 multiplexer? a) 2 b) 6 **c) 8** d) 5	L5

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49	Which IC is used for the implementation of 1-to-16 DEMUX? **a) IC 74154** b) IC 74155 c) IC 74139 d) IC 74138	L2
50	How many inputs will a decimal-to-BCD encoder have? a) 4 b) 8 **c) 10** d) 16	L2
51	How many outputs will a decimal-to-BCD encoder have? **a) 4** b) 8 c) 12 d) 16	L2
52	How is an encoder different from a decoder? **a) The output of an encoder is a binary code for 1-of-N input** b) The output of a decoder is a binary code for 1-of-N input c) The output of an encoder is a binary code for N-of-1 output d) The output of a decoder is a binary code for N-of-1 output	L3
53	If we record any music in any recorder, such types of process is called _____ a) Multiplexing **b) Encoding** c) Decoding d) Demultiplexing	L1
54	Can an encoder be a transducer? **a) Yes** b) No c) May or may not be d) Both are not even related slightly	L1
55	The discrepancy of 0 output due to all inputs being 0 or D0, being 0 is resolved by using additional input known as _____ **a) Enable** b) Disable c) Strobe d) Clock	L1
56	If two inputs are active on a priority encoder, which will be coded on the output? **a) The higher value** b) The lower value c) Neither of the inputs d) Both of the inputs	L2
57	Use the weighting factors to convert the following BCD numbers to binary _____	L2

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	0101 0011 & 0010 0110 1000 a) 01010011 001001101000 b) 11010100 100001100000 **c) 110101 100001100** d) 101011 001100001	
58	The primary use for Gray code is _____ **a) Coded representation of a shaft's mechanical position** b) Turning on/off software switches c) To represent the correct ASCII code to indicate the angular position of a shaft on rotating machinery d) To convert the angular position of a shaft on rotating machinery into hexadecimal code	L3
59	One way to convert BCD to binary using the hardware approach is _____ **a) With MSI IC circuits** b) With a keyboard encoder c) With an ALU d) UART	L2
60	Why is the Gray code more practical to use when coding the position of a rotating shaft? a) All digits change between counts b) Two digits change between counts **c) Only one digit changes between counts** d) Alternate digit changes between counts	L3
61	Reflected binary code is also known as _____ a) BCD code b) Binary code c) ASCII code **d) Gray Code**	L2
62	Why do we use gray codes? a) To count the no of bits changes b) To rotate a shaft **c) Error correction** d) Error Detetction	L2
63	Earlier, reflected binary codes were applied to _____ a) Binary addition b) 2's complement **c) Mathematical puzzles** d) Binary multiplication	L2
64	The binary representation of BCD number 00101001 (decimal 29) is _____ **a) 0011101** b) 0110101 c) 1101001 d) 0101011	L4

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65	Convert binary number into gray code: 100101. a) 101101 b) 001110 **c) 110111** d) 111001	L4
66	How many inputs will a decimal-to-BCD encoder have? a) 4 b) 8 **c) 10** d) 16	L2
67	How many outputs will a decimal-to-BCD encoder have? **a) 4** b) 8 c) 12 d) 16	L2
68	How is an encoder different from a decoder? **a) The output of an encoder is a binary code for 1-of-N input** b) The output of a decoder is a binary code for 1-of-N input c) The output of an encoder is a binary code for N-of-1 output d) The output of a decoder is a binary code for N-of-1 output	L2
69	How many OR gates are required for a Decimal-to-bcd encoder? a) 2 b) 10 c) 3 **d) 4**	L2
70	For 8-bit input encoder how many combinations are possible? a) 8 **b) 2^8** c) 4 d) 2^4	L3
71	The discrepancy of 0 output due to all inputs being 0 or D0, being 0 is resolved by using additional input known as _____ **a) Enable** b) Disable c) Strobe d) Clock	L3
72	If two inputs are active on a priority encoder, which will be coded on the output? **a) The higher value** b) The lower value c) Neither of the inputs d) Both of the inputs	L2