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Unit No : 3	**Unit Name : SYNCHRONOUS SEQUENTIAL CIRCUITS**	Date	30.09.2020

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S. No.	Objective Questions (MCQ /True or False / Fill up with Choices)	BTL
1	A latch is an example of a _____ a) Monostable multivibrator b) Astable multivibrator **c) Bistable multivibrator** d) 555 time	L1
2	Latch is a device with _____ a) One stable state **b) Two stable state** c) Three stable state d) Infinite stable states	L1
3	Why latches are called a memory devices? a) It has capability to stare 8 bits of data b) It has internal memory of 4 bit **c) It can store one bit of data** d) It can store infinite amount of data	L1
4	Two stable states of latches are _____ a) Astable & Monostable b) Low input & high output **c) High output & low output** d) Low output & high input	L1
5	How many types of latches are _____ **a) 4** b) 3 c) 2 d) 5	L2
6	The SR latch consists of _____ a) 1 input b) 2 inputs c) 3 inputs d) 4 inputs	L2
7	The outputs of SR latch are _____ a) x and y b) a and b c) s and r **d) q and q'**	L2
8	The NAND latch works when both inputs are _____ **a) 1** b) 0 c) Inverted d) Don't cares	L2
9	The inputs of SR latch are _____ a) x and y b) a and b	L1

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	c) s and r d) j and k	
10	When both inputs of SR latches are low, the latch _____ a) Q output goes high b) Q' output goes high **c) It remains in its previously set or reset state** d) it goes to its next set or reset state	L2
11	When both inputs of SR latches are high, the latch goes _____ a) Unstable b) Stable **c) Metastable** d) Bistable	L1
12	One example of the use of an S-R flip-flop is as _____ a) Transition pulse generator b) Racer **c) Switch debouncer** d) Astable oscillator	L1
13	When both inputs of a J-K flip-flop cycle, the output will _____ a) Be invalid b) Change **c) Not change** d) Toggle	L2
14	Which of the following is correct for a gated D-type flip-flop? **a) The Q output is either SET or RESET as soon as the D input goes HIGH or LOW** b) The output complement follows the input when enabled c) Only one of the inputs can be HIGH at a time d) The output toggles if one of the inputs is held HIGH	L1
15	A basic S-R flip-flop can be constructed by cross-coupling of which basic logic gates? a) AND or OR gates b) XOR or XNOR gates **c) NOR or NAND gates** d) AND or NOR gates	L1
16	In S-R flip-flop, if Q = 0 the output is said to be _____ a) Set **b) Reset** c) Previous state d) Current state	L2
17	The output of latches will remain in set/reset untill _____ **a) The trigger pulse is given to change the state** b) Any pulse given to go into previous state c) They don't get any pulse more d) The pulse is edge-triggered	L1
18	What is a trigger pulse?	L1

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	a) A pulse that starts a cycle of operation b) A pulse that reverses the cycle of operation c) A pulse that prevents a cycle of operation d) A pulse that enhances a cycle of operation	
19	What is an ambiguous condition in a NAND based S'-R' latch? a) S'=0, R'=1 b) S'=1, R'=0 c) S'=1, R'=1 **d) S'=0, R'=0**	L2
20	In a NAND based S'-R' latch, if S'=1 & R'=1 then the state of the latch is _____ **a) No change** b) Set c) Reset d) Forbidden	L2
21	One major difference between a NAND based S'-R' latch & a NOR based S-R latch is _____ **a) The inputs of NOR latch are 0 but 1 for NAND latch** b) The inputs of NOR latch are 1 but 0 for NAND latch c) The output of NAND latch becomes set if S'=0 & R'=1 and vice versa for NOR latch d) The output of NOR latch is 1 but 0 for NAND latch	L2
22	The characteristic equation of S-R latch is _____ **a) Q(n+1) = (S + Q(n))R'** b) Q(n+1) = SR + Q(n)R c) Q(n+1) = S'R + Q(n)R d) Q(n+1) = S'R + Q'(n)R	L2
23	The difference between a flip-flop & latch is _____ a) Both are same b) Flip-flop consist of an extra output **c) Latches has one input but flip-flop has two** d) Latch has two inputs but flip-flop has one	L1
24	One example of the use of an S-R flip-flop is as _____ a) Racer b) Stable oscillator **c) Binary storage register** d) Transition pulse generator	L2
25	On a positive edge-triggered S-R flip-flop, the outputs reflect the input condition when _____ a) The clock pulse is LOW b) The clock pulse is HIGH **c) The clock pulse transitions from LOW to HIGH** d) The clock pulse transitions from HIGH to LOW	L3
25	The circuit that is primarily responsible for certain flip-flops to be designated as edge-triggered is the _____	L2

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	a) Edge-detection circuit b) NOR latch c) NAND latch d) Pulse-steering circuit	
26	Which circuit is generated from D flip-flop due to addition of an inverter by causing reduction in the number of inputs? a) Gated JK-latch b) Gated SR-latch c) Gated T-latch **d) Gated D-latch**	L2
27	The characteristic of J-K flip-flop is similar to _____ **a) S-R flip-flop** b) D flip-flop c) T flip-flop d) Gated T flip-flop	L2
28	A J-K flip-flop can be obtained from the clocked S-R flip-flop by augmenting _____ **a) Two AND gates** b) Two NAND gates c) Two NOT gates d) Two OR gates	L3
29	How is a J-K flip-flop made to toggle? a) J = 0, K = 0 b) J = 1, K = 0 c) J = 0, K = 1 **d) J = 1, K = 1**	L2
30	The phenomenon of interpreting unwanted signals on J and K while Cp (clock pulse) is HIGH is called _____ a) Parity error checking **b) Ones catching** c) Digital discrimination d) Digital filtering	L2
31	In J-K flip-flop, “no change” condition appears when _____ a) J = 1, K = 1 b) J = 1, K = 0 c) J = 0, K = 1 **d) J = 0, K = 0**	L2
32	A J-K flip-flop with J = 1 and K = 1 has a 20 kHz clock input. The Q output is _____ a) Constantly LOW b) Constantly HIGH c) A 20 kHz square wave **d) A 10 kHz square wave**	L2
33	What is the significance of the J and K terminals on the J-K flip-flop? a) There is no known significance in their designations	L3

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	b) The J represents "jump," which is how the Q output reacts whenever the clock goes high and the J input is also HIGH **c) The letters were chosen in honour of Jack Kilby, the inventory of the integrated circuit** d) All of the other letters of the alphabet are already in use	
34	Two J-K flip-flops with their J-K inputs tied HIGH are cascaded to be used as counters. After four input clock pulses, the binary count is _____ **a) 00** b) 11 c) 01 d) 10	L3
35	Four J-K flip-flops are cascaded with their J-K inputs tied HIGH. If the input frequency (fin) to the first flip-flop is 32 kHz, the output frequency (fout) is _____ a) 1 kHz **b) 2 kHz** c) 4 kHz d) 16 kHz	L4
36	Determine the output frequency for a frequency division circuit that contains 12 flip-flops with an input clock frequency of 20.48 MHz. a) 10.24 kHz **b) 5 kHz** c) 30.24 kHz d) 15 kHz	L4
37	How many flip-flops are in the 7475 IC? a) 2 b) 1 **c) 4** d) 8	L2
38	In D flip-flop, D stands for _____ a) Distant **b) Data** c) Desired d) Delay	L1
39	The D flip-flop has _____ input. **a) 1** b) 2 c) 3 d) 4	L1
40	A D flip-flop can be constructed from an _____ flip-flop. **a) S-R** b) J-K c) T d) S-K	L2
41	In D flip-flop, if clock input is LOW, the D input _____	L2

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	a) Has no effect b) Goes high c) Goes low d) Has effect	
42	The D flip-flop has _____ input. **a) 1** b) 2 c) 3 d) 4	L2
43	Which statement describes the BEST operation of a negative-edge-triggered D flip-flop? **a) The logic level at the D input is transferred to Q on NGT of CLK** b) The Q output is ALWAYS identical to the CLK input if the D input is HIGH c) The Q output is ALWAYS identical to the D input when CLK = PGT d) The Q output is ALWAYS identical to the D input	L3
44	With regard to a D latch _____ a) The Q output follows the D input when EN is LOW b) The Q output is opposite the D input when EN is LOW **c) The Q output follows the D input when EN is HIGH** d) The Q output is HIGH regardless of EN's input state	L3
45	Which of the following is correct for a D latch? a) The output toggles if one of the inputs is held HIGH **b) Q output follows the input D when the enable is HIGH** c) Only one of the inputs can be HIGH at a time d) The output complement follows the input when enabled	L3
46	A D flip-flop utilizing a PGT clock is in the CLEAR state. Which of the following input actions will cause it to change states? a) CLK = NGT, D = 0 b) CLK = PGT, D = 0 c) CLOCK NGT, D = 1 **d) CLOCK PGT, D = 1**	L4
47	Why do the D flip-flops receive its designation or nomenclature as 'Data Flip-flops'? a) Due to its capability to receive data from flip-flop b) Due to its capability to store data in flip-flop **c) Due to its capability to transfer the data into flip-flop** d) Due to erasing the data from the flip-flop	L2
48	The characteristic equation of J-K flip-flop is _____ a) Q(n+1)=JQ(n)+K'Q(n) b) Q(n+1)=J'Q(n)+KQ'(n) c) Q(n+1)=JQ'(n)+KQ(n) **d) Q(n+1)=JQ'(n)+K'Q(n)**	L2
49	In a J-K flip-flop, if J=K the resulting flip-flop is referred to as _____ a) D flip-flop b) S-R flip-flop	L2

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	c) T flip-flop d) S-K flip-flop	
50	The only difference between a combinational circuit and a flip-flop is that _____ a) The flip-flop requires previous state b) The flip-flop requires next state **c) The flip-flop requires a clock pulse** d) The flip-flop depends on the past as well as present states	L2
51	The S-R latch composed of NAND gates is called an active low circuit because _____ a) It is only activated by a positive level trigger **b) It is only activated by a negative level trigger** c) It is only activated by either a positive or negative level trigger d) It is only activated by sinusoidal trigger	L3
52	Both the J-K & the T flip-flop are derived from the basic _____ a) S-R flip-flop **b) S-R latch** c) D latch d) D flip-flop	L2
53	The flip-flops which has not any invalid states are _____ a) S-R, J-K, D b) S-R, J-K, T c) J-K, D, S-R **d) J-K, D, T**	L2
54	What does the circle on the clock input of a J-K flip-flop mean? a) Level enabled b) Positive edge triggered **c) negative edge triggered** d) Level triggered	L2
55	On a positive edge-triggered S-R flip-flop, the outputs reflect the input condition when _____ a) The clock pulse is LOW b) The clock pulse is HIGH **c) The clock pulse transitions from LOW to HIGH** d) The clock pulse transitions from HIGH to LOW	L2
56	The asynchronous input can be used to set the flip-flop to the _____ a) 1 state b) 0 state **c) either 1 or 0 state** d) forbidden State	L2
57	Input clock of RS flip-flop is given to _____ a) Input **b) Pulser** c) Output	L2

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	d) Master slave flip-flop	
58	In JK flip flop same input, i.e. at a particular time or during a clock pulse, the output will oscillate back and forth between 0 and 1. At the end of the clock pulse the value of output Q is uncertain. The situation is referred to as? a) Conversion condition **b) Race around condition** c) Lock out state d) Forbidden State	L4
59	In a positive edge triggered JK flip flop, a low J and low K produces? a) High state b) Low state c) Toggle state **d) No Change State**	L2
60	If one wants to design a binary counter, the preferred type of flip-flop is _____ a) D type b) S-R type c) Latch **d) J-K type**	L3
61	S-R type flip-flop can be converted into D type flip-flop if S is connected to R through _____ a) OR Gate b) AND Gate **c) Inverter** d) Full Adder	L3
62	The term synchronous means _____ a) The output changes state only when any of the input is triggered **b) The output changes state only when the clock input is triggered** c) The output changes state only when the input is reversed d) The output changes state only when the input follows it	L3
63	The S-R, J-K and D inputs are called _____ a) Asynchronous inputs **b) Synchronous inputs** c) Bidirectional inputs d) Unidirectional inputs	L2
64	To realise one flip-flop using another flip-flop along with a combinational circuit, known as _____ a) PREVIOUS state decoder **b) NEXT state decoder** c) MIDDLE state decoder d) PRESENT state decoder	L2
65	For realisation of JK flip-flop from SR flip-flop, the input J and K will be given as _____ **a) External inputs to S and R**	L2

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	b) Internal inputs to S and R c) External inputs to combinational circuit d) Internal inputs to combinational circuit	
66	For realisation of JK flip-flop from SR flip-flop, if J=0 & K=0 then the input is _____ a) S=0, R=0 **b) S=0, R=X** c) S=X, R=0 d) S=X, R=X	L5
67	For realisation of JK flip-flop from SR flip-flop, if J=1, K=0 & present state is 0(i.e. Q(n)=0) then excitation input will be _____ a) S=0, R=1 b) S=X, R=0 **c) S=1, R=0** d) S=1, R=1	L5
68	For realisation of SR flip-flop from JK flip-flop, if S=1, R=0 & present state is 0 then next state will be _____ **a) 1** b) 0 c) Don't care d) Toggle	L6
69	The K-map simplification for realisation of SR flip-flop from JK flip-flop is _____ a) J=1, K=0 b) J=R, K=S **c) J=S, K=R** d) J=0, K=1	L5
70	For D flip-flop to JK flip-flop, the characteristics equation is given by _____ **a) D=JQ(p)'+Q(p)K'** b) D=JQ(p)'+KQ(p)' c) D=JQ(p)+Q(p)K' d) D=J'Q(p)+Q(p)K	L5
71	What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops? a) 0 to 2^n b) 0 to $2^n + 1$ **c) 0 to $2^n - 1$** d) 0 to $2^{n+1/2}$	L5
72	A decimal counter has _____ states. a) 5 **b) 10** c) 15 d) 20	L2
73	BCD counter is also known as _____ a) Parallel counter	L2

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	b) Decade counter c) Synchronous counter d) VLSI counter	
74	The parallel outputs of a counter circuit represent the _____ a) Parallel data word b) Clock frequency c) Counter modulus **d) Clock count**	L2
75	How many natural states will there be in a 4-bit ripple counter? a) 4 b) 8 **c) 16** d) 32	L2
76	One of the major drawbacks to the use of asynchronous counters is that _____ a) Low-frequency applications are limited because of internal propagation delays **b) High-frequency applications are limited because of internal propagation delays** c) Asynchronous counters do not have major drawbacks and are suitable for use in high- and low-frequency counting applications d) Asynchronous counters do not have propagation delays, which limits their use in high-frequency applications	L2
77	The terminal count of a typical modulus-10 binary counter is _____ a) 0000 b) 1010 **c) 1001** d) 1111	L4
78	Three cascaded decade counters will divide the input frequency by _____ a) 10 b) 20 c) 100 **d) 1000**	L5
79	A 4-bit counter has a maximum modulus of _____ a) 3 b) 6 c) 8 **d) 16**	L4
80	How many different states does a 3-bit asynchronous down counter have? a) 2 b) 4 c) 6 **d) 8**	L2
81	In a 3-bit asynchronous down counter, the initial content is _____ **a) 000** b) 111	L3

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	c) 010 d) 101	
82	In a 3-bit asynchronous down counter, at the first negative transition of the clock, the counter content becomes _____ a) 000 **b) 111** c) 101 d) 010	L3
83	In DOWN-counter, each flip-flop is triggered by _____ a) The output of the next flip-flop b) The normal output of the preceding flip-flop c) The clock pulse of the previous flip-flop **d) The inverted output of the preceding flip-flop**	L3
84	How can parallel data be taken out of a shift register simultaneously? a) Use the Q output of the first FF b) Use the Q output of the last FF c) Tie all of the Q outputs together **d) Use the Q output of each FF**	L4
85	The group of bits 11001 is serially shifted (right-most bit first) into a 5-bit parallel output shift register with an initial state 01110. After three clock pulses, the register contains _____ a) 01110 b) 00001 **c) 00101** d) 00110	L4
86	Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first) a) 1100 b) 0011 **c) 0000** d) 1111	L4
87	A serial in/parallel out, 4-bit shift register initially contains all 1s. The data nibble 0111 is waiting to enter. After four clock pulses, the register contains _____ a) 0000 b) 1111 **c) 0111** d) 1000	L5