Course/Branch : BE / EEE	**Year / Semester** : III / V	Format No.	NAC/TLP-07a.13
Subject Code :EE8551	**Subject Name** :Microprocessors and Microcontrollers	Rev. No.	02
Unit No : 04	**Unit Name :** Peripheral Interfacing	Date	30.09.2020

OBJECTIVE TYPE QUESTION BANK

S. No.	Objective Questions (MCQ /True or False / Fill up with Choices)	BTL
1	SPI device communicates in _____ **A) Simplex** B) Half duplex C) Full duplex D) Both half and full duplex	L1
2	Secure digital card application uses which protocol? A) UART **B) SPI** C) I2C D) USART	L2
3	Do SPI have/has a single master? **A) True** B) False	L1
4	How many logic signals are there in SPI? **A) 5 signals** B) 6 signals C) 4 signals D) 7 signals	L3
5	Port C of 8255 can function independently as A) input port B) output port **C) either input or output ports** D) both input and output ports	L2
6	The data bus buffer is controlled by A) control word register **B) read/write control logic** C) data bus D) none of the mentioned	L3

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7	SPI is described as Asynchronous serial interface. A) True **B) False**	L1
8	Which of the following is an advantage of SPI? **A) No start and stop bits** B) Use 4 wires C) Allows for single master D) Error checking is not present	L2
9	SMBUS stands for _____ A) Serial Memory Bus B) Serial Management Bus **C) System Management Bus** D) System Memory Bus	L3
10	Programmable peripheral input-output port is another name for A) serial input-output port **B) parallel input-output port** C) serial input port D) parallel output port	L2
11	All the functions of the ports of 8255 are achieved by programming the bits of an internal register called A) data bus control B) read logic control **C) control word register** D) none of the mentioned	L1
12	The input provided by the microprocessor to the read/write control logic is A) RESET B) A1 C) WR(ACTIVE LOW) **D) All of the mentioned**	L1
13	Which has a half duplex communication?	L1

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	A) Queued SPI **B) Micro wire** C) Micro wire/plus D) Quad SPI	
14	The device that receives or transmits data upon the execution of input or output instructions by the microprocessor is A) control word register B) read/write control logic **C) 3-state bidirectional buffer** D) none of the mentioned	L1
15	The port th1at is used for the generation of handshake lines in mode 1 or mode 2 is A) port A B) port B C) port C Lower **D) port C Upper**	L2
16	If A1=0, A0=1 then the input read cycle is performed from A) port A to data bus B) port B to data bus **C) port C to data bus** D) CWR to data bus	L1
17	The function, 'data bus tristated' is performed when A) CS(active low) = 1 B) CS(active low) = 0 C) CS(active low) = 0, RD(active low) = 1, WR(active low) = 1 **D) CS(active low) = 1 OR CS(active low) = 0, RD(active low) = 1, WR(active low) = 1**	L3
18	The pin that clears the control word register of 8255 when enabled is A) CLEAR B) SET **C) RESET** D) CLK	L1

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19	Which of the following depends the number of bits that are transferred? A) wait statement B) ready statement **C) time** D) counter	L1
20	What does SPI stand for? **A) serial parallel interface** B) serial peripheral interface C) sequential peripheral interface D) sequential port interface	L2
21	In which register does the data is written in the master device? **A) index register** B) Accumulator C) SPDR D) status register	L2
22	Which signal is used to select the slave in the serial peripheral interfacing? A) slave select B) master select **C) Interrupt** D) clock signal	L1
23	How much time period is necessary for the slave to receive the interrupt and transfer the data? A) 4 clock time period **B) 8 clock time period** C) 16 clock time period D) 24 clock time period	L2
24	How many pins does the 8255 PPI IC contains? A) 24 B) 20 C) 32 D) **40**	L3

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25	Which of the following pins are responsible for handling the on the Read Write control logic unit of the 8255 PPI? A) CS' B) RD' C) WR' **D) All of the above**	L1
26	In mode 2 of I/O mode, which of the following ports are capable of transferring the data in both the directions? **A) Port A** B) Port B C) Port C D) All of the above	L2
27	The _____ is a general purpose programmable I/O device designed to transfer the data from I/O to interrupt I/O. A) 8285A B) 8241A **C) 8255A** D) 8251A	L1
28	How many ports 8255A has? A) 2 **B) 3** C) 4 D) 5	L3
29	Which port can be split into two parts? A) PORT A B) PORT B **C) PORT C** D) PORT D	L1
30	How many bits of data can be transferred between the 8255 PPI and the interfaced device at a time? or What is the size of internal bus of the 8255 PPI? A) 16 bits B) 12 bits	L2

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	C) 8 bits D) None of the above	
31	INTR, WR signal is an input/output signal pin? A) both are output **B)** both are input **C) one is input and the other is output** D) none of the mentioned	L1
32	Which of the following uses N-MOS technology? A) 8253 B) 8254 C) 8255 **D) 8256**	L3
33	8 input DAC has _____ **A) 8 discrete voltage levels** B) 64 discrete voltage levels C) 124 discrete voltage levels D) 256 discrete voltage levels	L1
34	8253/54 can be operated in _____ Modes? A) 3 B) 4 C) 5 **D) 6**	L1
35	Which of the following statements are true about DAC0808? **A) parallel digital data to analog data conversion** B) it has current as an output C) all of the mentioned D) none of the mentioned	L2
36	All the functions of the ports of 8255 are achieved by programming the bits of an internal register called A) data bus control	L1

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	B) read logic control C) control word register **D) none of the mentioned**	