Course/Branch : B.E/EEE	**Year / Semester** : II/03	Format No.	NAC/TLP-07a.13
Subject Code : EE8351	**Subject Name** : DIGITAL LOGIC CIRCUITS	Rev. No.	02
Unit No : 5	**Unit Name : VHDL**	Date	30.09.2020

OBJECTIVE TYPE QUESTION BANK

S. No.	Objective Questions (MCQ /True or False / Fill up with Choices)	BTL
1	Which of the following is the basic building block of a design? a) Architecture **b) Entity** c) Process d) Package	L1
2	Complete description of the circuit to be designed is given in _____ **a) Architecture** b) Entity c) Library d) Configurations	L2
3	An entity can have more than one architecture. **a) True** b) False	L1
4	What is the use of Generics in VHDL? a) To turn on and off the drivers **b) To pass information to the entity** c) To describe architecture d) To divide code into small processes	L1
5	Which of the following describes the structure of VHDL code correctly? **a) Library Declaration; Entity Declaration; Architecture Declaration; Configurations** b) Entity Declaration; Configuration; Library Declaration; Architecture Declaration c) Configuration; Library Declaration; Entity Declaration; Architecture Declaration d) Library Declaration; Configuration; Entity Declaration; Architecture Declaration	L2
6	Which of the following is not defined by the entity? a) Direction of any signal b) Names of signal c) Different ports **d) Behavior of the signals**	L1
7	Which of the following can be the name of an entity? a) NAND **b) Nand_gate** c) Nand gate d) AND	L3
8	The entity name ‘xyz’ and ‘XYZ’ will be treated the same. **a) True**	L3

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Unit No : 5	**Unit Name : VHDL**	Date	30.09.2020

OBJECTIVE TYPE QUESTION BANK

	b) False	
9	In an assignment statement, OUT signal can be used only to the _____ **a) Left of <= operator** b) Right of <= operator c) Any side of <= operator d) Right of := operator	L2
10	On which side of assignment operator, we can use the IN type signal? a) Left **b) Right** c) Both d) Can't be used	L3
11	What is the difference between OUT and BUFFER? a) BUFFER can't be used inside the entity for reading the value and OUT can be b) BUFFER can only be read whereas OUT can only be assigned a value **c) BUFFER can be read as well as assigned a value but OUT can only be assigned** d) Both are same	L3
12	How to control the structure and timing of the entity can be changed? a) By using TIME variable in the entity b) By changing the entity declaration from time to time c) By using some special code **d) By using GENERICS**	L2
13	Which of the following is the default mode for a port variable? **a) IN** b) OUT c) INOUT d) BUFFER	L2
14	What does the architecture of an entity define? a) External interface **b) Internal functionality** c) Ports of the entity d) Specifications	L1
15	What does the declarative part of architecture contain? a) Declaration of another entity b) Declaration of libraries and packages **c) Declaration of local signals, constants or subprograms** d) Declaration of Architecture type	L1
16	The statements in between the keyword BEGIN and END are called _____	L3

Course/Branch : B.E/EEE	**Year / Semester** : II/03	Format No.	NAC/TLP-07a.13
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Unit No : 5	**Unit Name : VHDL**	Date	30.09.2020

OBJECTIVE TYPE QUESTION BANK

	a) Concurrent statements b) Netlist c) Declaration statement d) Entity function	
17	Which of the following can't be declared in the declaration part of the architecture? a) Signals b) Subprograms c) Components **d) Libraries**	L1
18	SIGNED and UNSIGNED data types are defined in which package? a) std_logic_1164 package b) std_logic package **c) std_logic_arith package** d) standard package	L2
19	What is the correct method to declare a SIGNED type signal 'x'? a) SIGNAL x : IN SIGNED b) SIGNAL x : IN SIGNED **c) SIGNAL x : IN SIGNED (7 DOWNTO 0)** d) SIGNAL x : IN SIGNED_VECTOR (7 DOWNTO 0)	L2

20	Which of the following option is completely legal, given that a and b are two UNSIGNED type signals?
	
	a) x <= a + b; y <= a – b;
	b) x <= a OR b; y <= a AND b;
	c) x <= a + b; y <= a OR b;
	d) x <= a OR b; y <= a + b;
		L2

21	If a and b are two STD_LOGIC_VECTOR input signals, then legal assignment for a and b is? a) x <= a.b **b) x <= a OR b** c) x <= a + b d) x <= a && b	L2
22	SIGNAL a : REAL; which of the following is illegal assignment for a? a) a <= 1.8 b) a <= 1.0 E10 c) a <= 1.0 E-10 **d) a <=1.0 ns**	L3
23	What is the difference between SIGNAL and VARIABLE? a) The value of SIGNAL never varies whereas VARIABLE can change its value	L2

Course/Branch : B.E/EEE	**Year / Semester** : II/03	Format No.	NAC/TLP-07a.13
Subject Code : EE8351	**Subject Name** : DIGITAL LOGIC CIRCUITS	Rev. No.	02
Unit No : 5	**Unit Name : VHDL**	Date	30.09.2020

OBJECTIVE TYPE QUESTION BANK

	b) SIGNAL can be used for input or output whereas VARIABLE acts as intermediate signals c) SIGNAL depends upon VARIABLE for various operations **d) SIGNAL is global and VARIABLE is local to the process in which it is declared**	
24	Access types are similar to _____ in traditional programming languages. **a) Pointers** b) Arrays c) Structures d) Files	L2
25	A VARIABLE y is declared of STD_LOGIC_VECTOR type of 4 bits, if you want to assign 1001 to y, then what is the write assignment statement? a) y <= “1001” **b) y := “1001”** c) y <= ‘1’, ‘0’, ‘0’, ‘1’ d) y => “1001”	L4
25	Which of the following logical operator has the highest precedence? a) NAND b) NOR **c) NOT** d) EXOR	L2
26	Which of the following VHDL statement is equivalent to NAND operation, if y, a and b are SIGNALS? a) y <= NOT a AND b **b) y <= NOT a OR NOT b** c) y <<= NOT a AND NOT b d) y <<= NOT (a OR b)	
27	_____ operator is unary as well as binary operator. **a) –** b) * c) / d) **	L2
28	The operator ‘&’ is called the_____ operator. a) Logical AND operator b) Bitwise AND operator c) Arithmetic addition operator **d) Concatenation operator**	L2
29	The operators like =, /=, <, >, >= are called _____ a) Arithmetic operators	L2

Course/Branch : B.E/EEE	**Year / Semester** : II/03	Format No.	NAC/TLP-07a.13
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Unit No : 5	**Unit Name : VHDL**	Date	30.09.2020

OBJECTIVE TYPE QUESTION BANK

	b) Concatenation operators c) Logical operators **d) Relational operators**	
30	ABS operator is used to _____ a) Shift the operand **b) Gives absolute value for the operand** c) Give the result as nearest integer d) To synthesize the result	L1
31	What is the use of shift operators? **a) To shift the data** b) To shift the identifiers c) To shift the operators d) To shift the STD_LOGIC_VECTOR	L2
32	The correct syntax for any logical shift operator like SLL and SRL is_____ **a) bit_vector_operand <OPERATOR> integer_operand** b) integer_operand <OPERATOR> bit_vector_operand c) std_logic_operand <OPERATOR> integer_operand d) integer_operand <OPERATOR> std_logic_operand	L2
33	SLL operation is equivalent to which of the following operations? a) Multiplication by any natural number **b) Multiplication by 2** c) Division by 2 d) Exponential operation	L2
34	What is the use of simulation deltas in VHDL code? a) To create delays in simulation b) To assign values to signals **c) To order some events** d) Evaluate assignment statements	L2
35	Which function is used to create a single value for multiple driver signals? **a) Resolution function** b) Package c) Concurrent assignments d) Sequential assignments	
36	A signal is driven by two signals b and c. How the value of b and c will be resolved to calculate the value of a? **a) By short circuiting both driver** b) By open circuiting one driver c) By AND operation between two drivers d) By NOT operation of both drivers	L5

Course/Branch : B.E/EEE	**Year / Semester** : II/03	Format No.	NAC/TLP-07a.13
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Unit No : 5	**Unit Name : VHDL**	Date	30.09.2020

OBJECTIVE TYPE QUESTION BANK

37	Which of the following is default delay in VHDL? **a) Inertial delay** b) Transport delay c) Delta delay d) Wire delay	L2
38	A buffer with single input A and single output B has a delay of 20 nanosecond. If the value of input A changes after 10 ns from 0 to 1 and it changes again from 1 to 0 at 20 ns. At what time, the value of output B will be 1, if the inertial delay model is used? a) 30 ns b) 40 ns c) 20 ns **d) Output will remain zero**	L5
39	A buffer with single input A and single output B has a delay of 20 nanosecond. If the value of input A changes after 10 ns from 0 to 1 and it changes again from 1 to 0 at 20 ns. At what time, the value of output B will be 1, if the transport delay model is used? a) 20 ns **b) 30 ns** c) 40 ns d) Output will remain zero	L5
40	What do you mean by a block? a) An object of architecture b) Interconnection of two or more signals c) A part of an entity **d) A sub module in an architecture body**	L2
41	A procedure can't contain a _____ statement. a) WAIT b) IF **c) RETURN** d) CASE	L2
42	Which of the following defines the interface to the block? a) Block declaration part **b) Block header** c) Block statement part d) Generic declaration part	L2
43	What is the main purpose of using blocks? a) To improve reusability b) To improve conditional execution **c) To improve readability** d) To improve speed of execution	L1

Course/Branch : B.E/EEE	**Year / Semester** : II/03	Format No.	NAC/TLP-07a.13
Subject Code : EE8351	**Subject Name** : DIGITAL LOGIC CIRCUITS	Rev. No.	02
Unit No : 5	**Unit Name : VHDL**	Date	30.09.2020

OBJECTIVE TYPE QUESTION BANK

44	Which of the following is true about guarded blocks? a) Guarded blocks can have only guarded statements **b) Guarded blocks can have both guarded as well as unguarded statements** c) Guarded blocks are executed when guarded expression is false d) Guarded expression can have BIT type	L2
45	Which of the following is the use of IF generation? a) To handle repeating pattern of design **b) To handle exceptional cases of design** c) To design full adder circuit d) To connect input instances with output	L2
46	Which of the following is defined in structural modeling? **a) The structure of circuit** b) Behavior of circuit on different inputs c) Data flow from input to output d) Functional structure	L3
47	Which of the following is similar to the entity declaration in structural modeling? a) Component instantiation **b) Component declaration** c) Port map d) Generic map	L2
48	Which of the following is the correct syntax for component instantiation? a) instantiate : component_name PORT MAP (port_list); b) label : instantiate COMPONENT PORT MAP (port_list); **c) label : component_name PORT MAP (port_list);** d) label : instantiate component_name PORT MAP (port_list)	L2
49	Which of the following function is used to map the component? a) COMPONENT INSTANTIATE **b) PORT MAP** c) GENERIC MAP d) US	L2

50	A component has 3 ports- two inputs(a and b) and one output(y). Which of the following statement is for the positional mapping of the component?
	
	a) LABEL : my_component PORT MAP (l, m, n);
	b) LABEL : my_component PORT MAP (y, a);
	c) LABEL : my_component PORT MAP (l => a, m => b, n => y);
	d) LABEL : my_component PORT MAP(a, b, y>= a);
		L5

51	Which of the following is the right way to leave a port unconnected? a) L1 : my_component PORT MAP(a); a <= OPEN;	L2

Course/Branch : B.E/EEE	**Year / Semester** : II/03	Format No.	NAC/TLP-07a.13
Subject Code : EE8351	**Subject Name** : DIGITAL LOGIC CIRCUITS	Rev. No.	02
Unit No : 5	**Unit Name : VHDL**	Date	30.09.2020

OBJECTIVE TYPE QUESTION BANK

	b) L1 : my_component PORT MAP(a := OPEN);
	c) L1: my_component PORT MAP(a => OPEN);
	d) L1 : my_component PORT MAP(a); a := OPEN;	

52	Which of the following is the correct order for a structural model in VHDL? **a) Libraries, Entity declaration, Component declaration, Component instantiation** b) Libraries, Component declaration, Entity declaration, Component instantiation c) Libraries, Entity declaration, Component instantiation, Component declaration d) Component declaration, Libraries, Entity declaration, Component instantiation	L2
53	What is the correct syntax for mapping a GENERIC parameter in structural modeling? **a) label : component_name GENERIC MAP(parameter_list) PORT MAP(port_list)** b) label : component_name GENERIC MAP(parameter_list) c) label : parameter_name GENERIC MAP(parameter_list) PORT MAP(port_list) d) label : parameter_name GENERIC MAP(parameter_list) PORT MAP(port_list)	L2
54	A component instantiation statement generates a(n) _____ of the component. a) Class b) Behavior c) Structure **d) Object**	L1
55	How can we use an assignment statement as a sequential assignment? a) By using keyword WAIT b) By using a delay mechanism c) By using conditional statements **d) By using it in any process**	L2

56	Which of the following is correct syntax for a signal assignment statement (if {} specifies an optional part)?
	
	a) target <= {delay_mechanism} waveform;
	b) target <= delay_mechanism waveform;
	c) target <= delay_mechanism {waveform};
	d) target <= {delay_mechanism} {waveform} value;
		L3

57	Which of the following is a keyword used for conditional assignment? a) IF **b) WHEN** c) FOR d) END	L2

Course/Branch : B.E/EEE	**Year / Semester** : II/03	Format No.	NAC/TLP-07a.13
Subject Code : EE8351	**Subject Name** : DIGITAL LOGIC CIRCUITS	Rev. No.	02
Unit No : 5	**Unit Name : VHDL**	Date	30.09.2020

OBJECTIVE TYPE QUESTION BANK

58	The selected concurrent statement is equivalent to _____ sequential statement. a) If else b) Loop c) Wait **d) Case**	L1
59	Those statement which are placed under _____ are concurrent. a) Process b) Function **c) Architecture** d) Procedure	L1
60	Which of the following statement is a zero delay statement? a) y <= x AFTER 10 ns b) y <= TRANSPORT x AFTER 10 ns c) y <= x **d) y := x AFTER 10 ns**	L2
61	If there is more than one process in a VHDL code, How they are executed? a) One after the other **b) Concurrently** c) According to sensitivity list d) Sequentially	L3
62	What is the effect of the sensitivity list on the process? **a) Process executes when any of the signal in sensitivity list changes** b) Process executes sequentially when sensitivity list is specified c) If there is no sensitivity list, then the process will not execute d) Helps in simulation	L2
63	A _____ can't be declared inside a process. **a) Signal** b) Variable c) Constants d) Subprograms	L1
64	A postponed process runs when _____ **a) All the other processes have completed** b) After completion of one particular process c) Concurrently with all other processes d) First of all processes	L2
65	Which of the following statement can't be used inside a process? a) WAIT b) IF ELSE	L2

Course/Branch : B.E/EEE	**Year / Semester** : II/03	Format No.	NAC/TLP-07a.13
Subject Code : EE8351	**Subject Name** : DIGITAL LOGIC CIRCUITS	Rev. No.	02
Unit No : 5	**Unit Name : VHDL**	Date	30.09.2020

OBJECTIVE TYPE QUESTION BANK

	c) Variable declaration **d) PORT MAP**	
66	A loop statement is used where we needs to _____ a) Select one from many choices b) Check a condition **c) Repeat the statements** d) Choose one from two cases	L2
67	Loop is a _____ statement. a) Concurrent **b) Sequential** c) Assignment d) Functional	L1
68	What is the use of FOR loop? **a) To repeat the statement finite number of times** b) To repeat the statement until any condition holds true c) To repeat the statements for infinite time d) To repeat statements inside until any condition is false	L2
69	What does the next statement in loops do? **a) Skips the current iteration** b) Starts the next loop by ending the current c) Exits the loop d) Skips the next line of the loop	L1
70	What is the syntax to use the NEXT statement? a) NEXT condition loop_label **b) NEXT loop_label WHEN condition** c) loop_label NEXT WHEN condition d) loop_label NEXT condition	L1
71	The parameters used at the time of function call are called _____ a) Formal parameters **b) Actual parameters** c) Real parameters d) Complex parameters	L1
72	Which of the following could be the objects in the parameter list of a procedure? a) CONSTANTS, VARIABLES b) VARIABLES, SIGNALS c) CONSTANTS, SIGNALS **d) CONSTANT, SIGNALS, VARIABLES**	L2

Course/Branch : B.E/EEE	**Year / Semester** : II/03	Format No.	NAC/TLP-07a.13
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OBJECTIVE TYPE QUESTION BANK